WM8962-6243-CS49-M-REV2

Example Configurations

DOC TYPE:	EXAMPLE CONFIGURATIONS
BOARD REFERENCE:	WM8962-6243-CS49-M-REV2
BOARD TYPE:	Customer Mini Board
WOLFSON DEVICE(S):	WM8962
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INTRODUCTION

The WM8962-6243-CS49-M-REV2 Customer Mini Board is compatible with the 6243-EV1 customer main board and together provide a complete hardware platform for evaluation of the WM8962. The WM8962 Customer Mini Board can also be used independently and connected directly to a processor board using flying wires or appropriate headers. This document will cover both, but performance data will be based on the Wolfson system with 6243-EV1 main board. Configurations covered are listed below:

- Microphone IN1 to ADC (S/PDIF)
- Line IN1 to ADC (S/PDIF)
- Line IN2 to ADC (S/PDIF)
- Line IN1 to ADC (crystal oscillator)
- DAC to Headphones (FLL)
- DAC to Headphones (crystal oscillator)
- DAC to Speakers (FLL)

This document should be used as a starting point for evaluation of WM8962 but it will not cover every possible configuration.

Assumptions:

1. The user is familiar with the 6243-EV1 main board and that board is configured correctly for the path of interest (see related documents below).
2. The user has setup WISCE as per instruction and has control of the microhub (register settings provided in this document)
3. Device configuration text files for any given audio path comprise an initial startup part which configures clocking (e.g. Startup_48.000KHz_512Fs_MCLK.txt) and a second part which sets up the chosen audio path (e.g. WSEQ_DAC-HP_DCServo_0dB_volume.txt)

Related documents:

1. WM8962_6243_CS49_M_REV2_Schematic_Layout
2. 6243_EV1_REV1_Schematic_Layout
3. WISCE Quick Start Guide

For the configurations in this document, the audio interface is connected to the main board through the S/PDIF OPTICAL IN and S/PDIF OPTICAL OUT connectors. For the configuration where the Crystal Oscillator is used, the audio interface is run in master. All control signals for the device are using the 2-wire interface through the USB interface. All setup files are for 48KHz sample frequency using a reference MCLK frequency of 12.288MHz. The setup file for the Crystal Oscillator is for a 48KHz sample frequency using the on-chip PLL3 to generate the 24.576MHz frequency.

The SPDIF interface can only provide a clock of up to 12.288MHz, which translates to a clock rate of 256Fs for the 48KHz sample frequency example configurations presented in this manual. To facilitate the evaluation of the DSP2 Soundware™ features applicable to Headphones and Speakers, the on-chip FLL block has been used to provide the required 512Fs clock rate.

TERMINOLOGY

AIF	Audio Interface
USB	Universal Serial Bus
EVB	Evaluation Board
MCU	Microprocessor Control Unit
S/PDIF	Sony / Philips Digital Interface Format

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CONTROL INTERFACE SELECTION

The Control Interface of the WM8962 can operate in either 2-,3- or 4-wire mode. The 6243-EV1 main board is configured by default to use the 2-wire mode, however customers can select the 3-,4-wire mode by configuring the jumpers as described in Table 1 and by selecting the desired control interface mode in the WISCE software as shown in Figure 1.

For more information please refer to the Control Interface section of the WM8962 datasheet.

REF-DES	LINK STATUS	DESCRIPTION
J28 (CIFMODE)	2 - 3	2 wire or 3-4 wire selection mode is driven by WISCE as shown in Figure 1
J27 (GPIO2_SEL)	Link in place	GPIO2 used as SDOUT pin
J31 (GPIO6_SEL)	2 - 3	GPIO6 used as CSB pin

Table 1 Main Board 6243 Jumper Settings for 3-, 4-wire Control Interface Mode

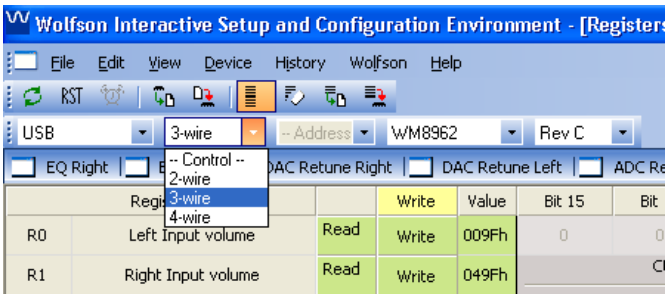


Figure 1 Control Interface Selection Mode in WISCE™

BOARD CONFIGURATION STAND-ALONE

The WM8962 Customer Mini Board can be used a stand-alone module for direct connection to a processor board via flying leads or dedicated headers. This section will detail important considerations and provide all information required to do this without risking damage to the device.

CONNECTION DIAGRAM

Figure 2 below shows the connections required to power-up and control the WM8962 Customer Mini Board. Please refer to the Table 2 for further detail on external I/O connections.

Pin GPIO5 must be tied to either DBVDD via a weak pull-up (logic 1) or ground (logic 0). It must not be left floating. Please refer to WAN_0248 for more information about the functionality of pin GPIO5.

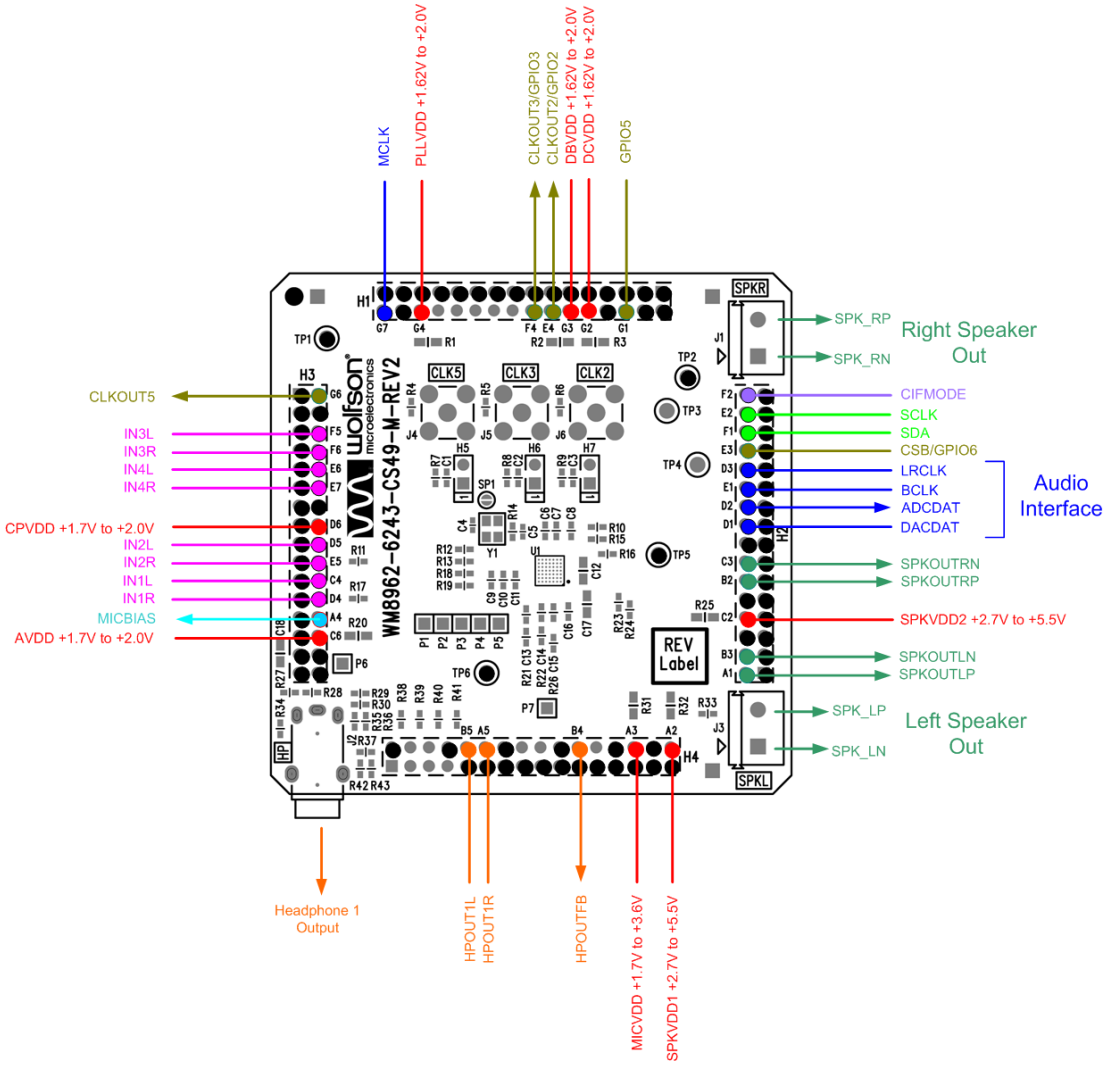


Figure 2 Stand-Alone Board Configuration

I/O TABLE

SIGNAL	BOARD REFERENCE	IMPORTANT NOTES
Voltage Supplies		
AVDD	D6	AVDD = 1.7V to 2.0V
DCVDD	G2	DCVDD = 1.7V to 2.0V
DBVDD	G3	DBVDD = 1.7V to 3.6V
CPVDD	C6	CPVDD = 1.7V to 2.0V
SPKVDD1	A2	SPKVDD1 = 1.7V to 5.5V
SPKVDD2	C2	SPKVDD2 = 1.7V to 5.5V
MICVDD	A3	MICVDD = 1.7V to 3.6V
PLLVDD	G4	PLLVDD = 1.7V to 2.0V
Ground		
AGND	Common GND on TP1, TP2, TP5 & TP6	Analogue and Digital grounds must always be within 0.3V of each other
DGND		
CPGND		
SPKGND1		
SPKGND2		
PLLGND		
Control Interface		
SCLK	F1	Controlled signals should be externally pulled high to DBVDD
SDA	E2	
Master Clock		
MCLK	G7	Clock should swing between DBVDD and DGND
Audio Interface		
BCLK	E1	Audio interface signals should swing between DBVDD and DGND
LRCLK	D3	
DACDAT	D1	
ADCDAT	D2	
Analogue Inputs		
IN1L	C4	Analogue input voltage should be between AGND and AVDD
IN1R	D4	
IN2L	D5	
IN2R	E5	
IN3L	F5	
IN3R	F6	
IN4L	E6	
IN4R	E7	
Analogue Outputs		
MICBIAS	A4	Microphone bias voltage
SPKOUTLP	SPK_L	Positive terminal of 8Ω BTL speaker (screw terminal) Note: remove jumper “SPK_L_LOAD” on 6243 mainboard when using external load
SPKOUTLN		Negative terminal of 8Ω BTL speaker (screw terminal) Note: remove jumper “SPK_L_LOAD” on 6243 mainboard when using external load
SPKOUTRP	SPK_R	Positive terminal of 8Ω BTL speaker (screw terminal)

SIGNAL	BOARD REFERENCE	IMPORTANT NOTES
		Note: remove jumper “SPK_R_LOAD” on 6243 mainboard when using external load
SPKOUTRN		Negative terminal of 8Ω BTL speaker (screw terminal) Note: remove jumper “SPK_R_LOAD” on 6243 mainboard when using external load
HPOUT1L	HP	Ground referenced headphone output – 3.5mm jack (left channel)
HPOUT1R		Ground referenced headphone output – 3.5mm jack (right channel)

Table 2 I/O Configuration

EXTERNAL MICROPHONE, ACCESSORY DETECT AND BUTTON DETECT CIRCUITS

The WM8962 Customer Mini Board can be configured for IN1L Microphone input, Multiple button detection via IN4L or Line input as defined in Table 3

	IN1L MICROPHONE INPUT	MULTIPLE BUTTON DETECTION	IN1 LINE INPUT
MICBIAS	Enabled (MICBIAS_ENA=1)	Enabled (MICBIAS_ENA=1)	Disabled (MICBIAS_ENA=0)
C18	populated	populated	unpop
R34	populated	populated	unpop
R28	populated	populated	unpop
Functionality	One button detection via MICBIAS threshold; microphone input supported via IN1L. (please refer to Figure 3)	Multiple button detection supported via IN4L; microphone input not supported. (please refer to Figure 4)	Button detection not supported

Table 3 IN1 to ADC Configurations Settings for Microphone Input or Line Input

IN1L MICROPHONE INPUT

By default the WM8962 Customer Mini Board is configured to support external microphone connection, the Accessory-detect and Button-detect functionality as shown in Figure 3.

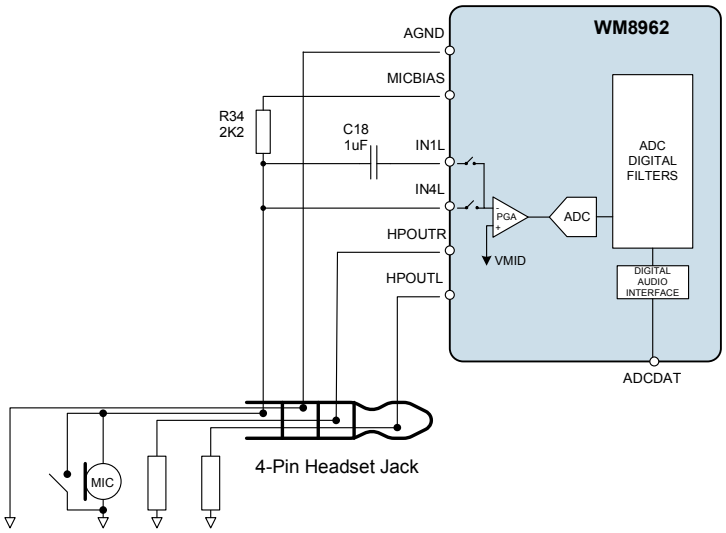


Figure 3 Default Configuration of the Headphone Output of the WM8962-6243-CS49-M-REV2 Customer Mini Board

For more information on the Headphone Output of the WM8962-6243-CS49-M-REV2 Customer Mini Board, and other 4-pin headset jack supported configurations, please refer to the WM8962_6243_CS49_M_REV2_Schematic_Layout document.

MULTIPLE BUTTON DETECTION

Multiple push button detection is supported using carefully chosen resistors as shown in Figure 4 to distinguish one push button from another, and by using the WM8962 Analogue to Digital Converter (ADC) to measure the potential divider formed between the MICBIAS resistor R34 and the push button resistors.

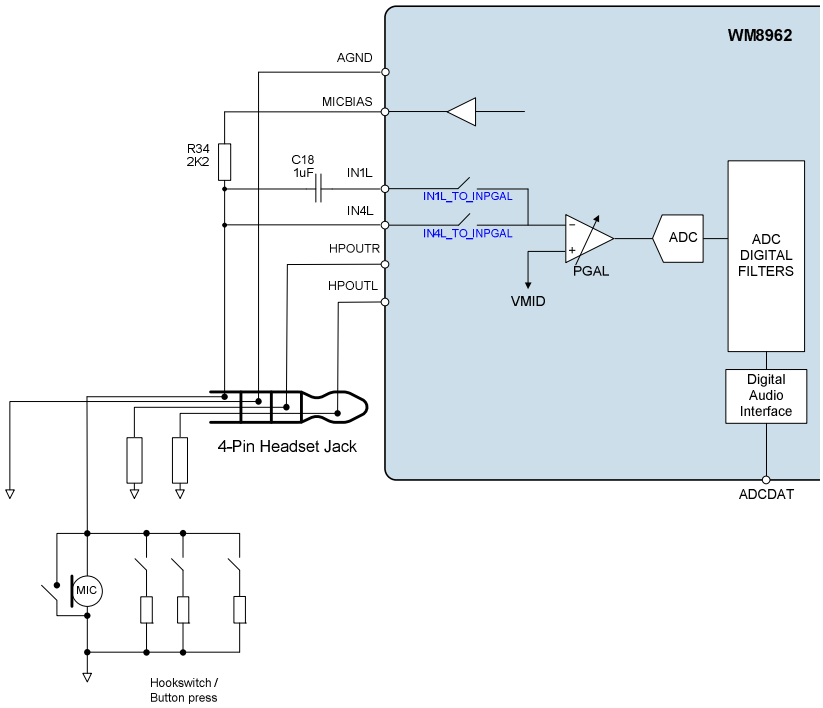


Figure 4 Reference Button-detect Circuitry

Multiple push button detection functionality relies on IN4L channel, therefore simultaneous microphone recording through IN1L channel is not supported.

To maximize the measurable voltage range, it is recommended that the IN4 to ADC path is set up with -6dB gain. In addition the input PGA and input mixer should be disabled and the ADC high pass filter turned off by writing to register ADC_HPF_DIS = 0 (address 0x05, bit 0). The ADC measured voltage can be calculated from the ADC output code using the following equation.

$$ADC_{Measured\ Voltage}(V) = \left[\frac{\left(\frac{ADC_{Input\ Range}\ (V)}{2}\right)}{2^{(ADC\ Resolution-1)bits}} \times ADC_{Output\ Code}(dec)\right] - ADC\ Offset(V)$$

For further information on the button detection functionality please refer to the Multiple Push Button Detection section of the WM8962 datasheet.

BOARD CONFIGURATION WITH 6243-EV1 MAIN BOARD

This section focuses on evaluation of the WM8962-6243-CS49-M-REV2 Customer Mini Board in combination with the 6243-EV1 main board. This system is the reference platform for measurement data contained in this document. Please note that only a limited number of usage modes will be covered.

MICROPHONE IN1 TO ADC

When C18 and R34 components are populated and MICBIAS enabled, the performance of Microphone IN1 to ADC path can be tested using the recommended setup shown in Figure 5. An ECM microphone is simulated by applying the input signal across a 10uF capacitor and 2.2kohms resistor connected between Pin 1 of Headset Jack and GND.

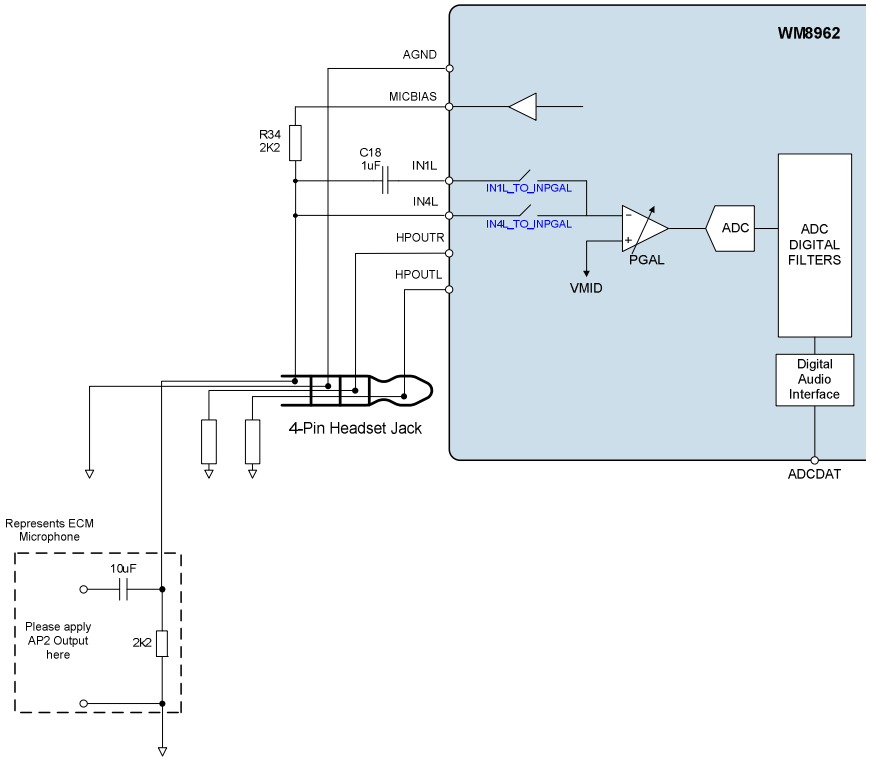
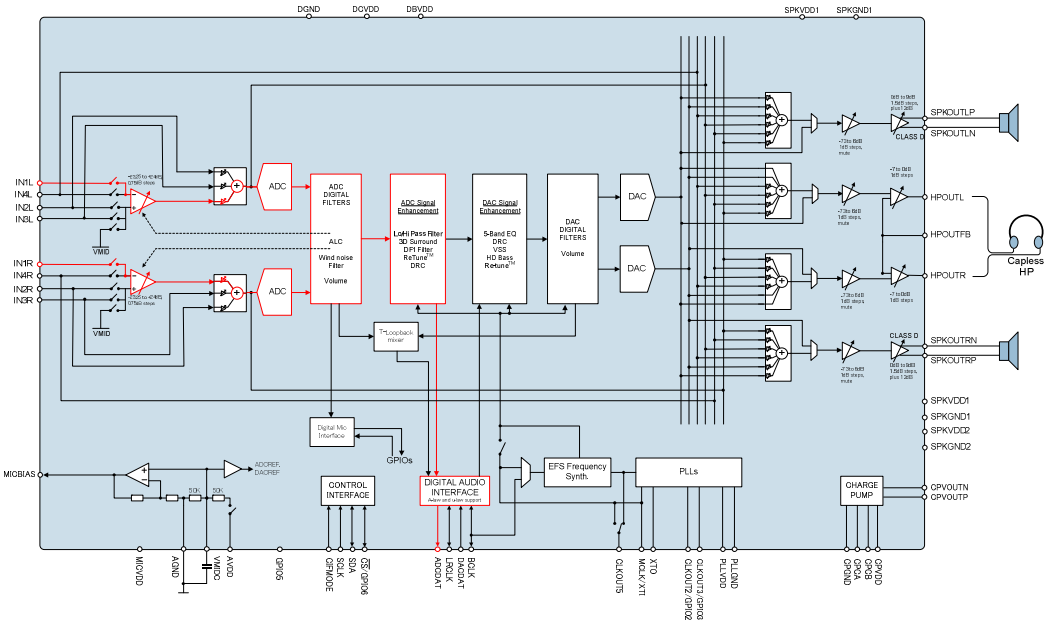


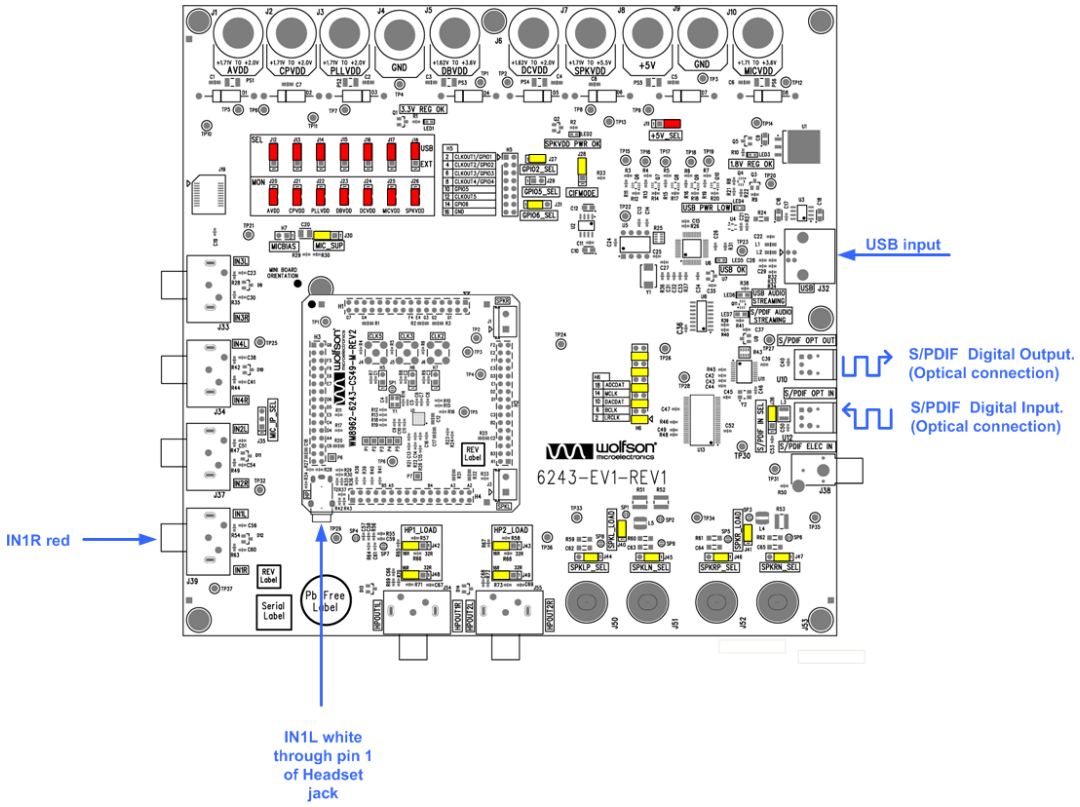
Figure 5 Reference Microphone IN1 to ADC Circuit

The following section details board configuration for Microphone IN1 to ADC.

BLOCK DIAGRAM



BOARD CONFIGURATION



JUMPERS	JUMPER STATUS	DESCRIPTION
J11, J12, J13, J14, J15, J16, J17, J18	2 – 3	**USB power supply selected for all supplies**
J20, J21, J22, J23, J24, J25, J26	Links fitted	**Monitoring supplies**
J36	2 – 3	**S/PDIF_IN_SEL** Select the S/PDIF optical input.
H6	1 – 2 5 – 6 9 – 10 13 – 14 17 – 18	**AIF Interface** These links needed for connection to external clock source and Digital Dout derived from the S/PDIF interface.
J42,J48	2 – 3	**Headphones 1 Loads** Select 16R load
J43,J49	2 – 3	**Headphones 2 Loads** Select 16R load
J44 J40	1 – 2 Link fitted	**SPK_LP_SEL** Left channel positive analogue output on J50 with 8.2Ω load and no filter.
J45	1 – 2	**SPK_LN_SEL** Left channel negative analogue output on J51 with 8.2Ω load and no filter.
J46 J41	1 – 2 Link fitted	**SPK_RP_SEL** Right channel positive analogue output on J52 with 8.2Ω load and no filter.
J47	1 – 2	**SPK_RN_SEL** Right channel negative analogue output on J53 with 8.2Ω load and no filter.
J27	Link fitted	**GPIO2_SEL**
J28	2 – 3	**CIFMODE**
J29	Link not fitted	**GPIO5_SEL**
J31	1 – 2	**GPIO6_SEL**
J30	2 – 3	**MICSUP**
H7	1: MICBIAS 2: GND	**MICBIAS** Microphone bias voltage output on H7
J35	Link not fitted	**MIC_IP_SEL**

Table 4 Main Board 6243 Jumper Settings for IN1 to ADC using Optical S/PDIF

REGISTER SETTINGS

Register settings provided below are the minimum requirement to configure the desired audio path.

REG INDEX	DATA VALUE	COMMENT
Clocking configuration for 48kHz @ 256Fs		
0x0F - write	0x0000	Software Reset
0x81 - write	0x0001	Define OSC_ENA=0, PLL2_ENA=0, PLL3_ENA=0
0x7D - write	0x0048	Define CLKOUT2_DIV=0, CLKOUT5_DIV=0
0x7C - write	0x0000	Define CLKOUT3_SEL=00, CLKOUT5_SEL=0
0x08 - write	0x09C4	Set CLKREG_OVD=1 (clocking registers are controlled by the Control Interface), Disable system clock (SYSCLK_ENA = 0), Set system clock source to MCLK
0x38 - write	0x0506	Set MCLK_RATE to 256*Fs
0x1B - write	0x0010	Set SAMPLE_RATE to 48KHz
0x08 - write	0x09E4	Re-Enable system clock (SYSCLK_ENA=1), Ensure clocking registers are controlled normally via Control Interface (CLKREG_OVD=1)
0x1C - write	0x0018	Enable current bias circuits
0x19 - write	0x01C0	Bring up VMID quickly, enable master bias
Wait 4.5 ms		
IN1 to ADC audio path setup using Write Sequencer		
0x25 - write	0x0008	Set IN1L_TO_INPGAL=1
0x26 - write	0x0008	Set IN1R_TO_INPGAR=1
0x00 - write	0x011F	Unmute input left PGAs by setting INPGAL_MUTE=0, set 0dB volume
0x01 - write	0x011F	Unmute input right PGAs by setting INPGAR_MUTE=0, set 0dB volume
0x57 - write	0x0020	Enable write sequencer
0x5A - write	0x0092	Start write sequencer
Wait 150 ms for the Write Sequencer to finish		
0x5D - read	-	Read status of write sequencer to check that WSEQ CURRENT INDEX = 0000000 and WSEQ_BUSY = 0

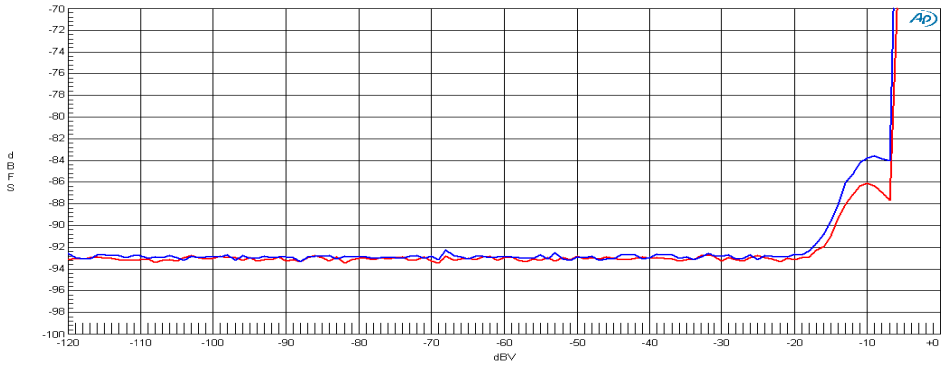
PERFORMANCE PLOT

AVDD = CPVDD = PLLVDD = DBVDD = DCVDD = 1.8V; SPKVDD = 5V; MICVDD = 2.5V

Sample Frequency = 48KHz

THD+N Amplitude (A-weighted)

WM8962 ADC – THD+N v Amplitude – Microphone IN1 to ADC – Slave mode 256Fs – Reference Microphone IN1 to ADC circuitry of Figure 5 being used and C18, R34 and R28 populated – IN1L driven from circuitry of Figure 5, IN1R driven from Phono connector J39 on to the 6243-EV1-REV1 main board.

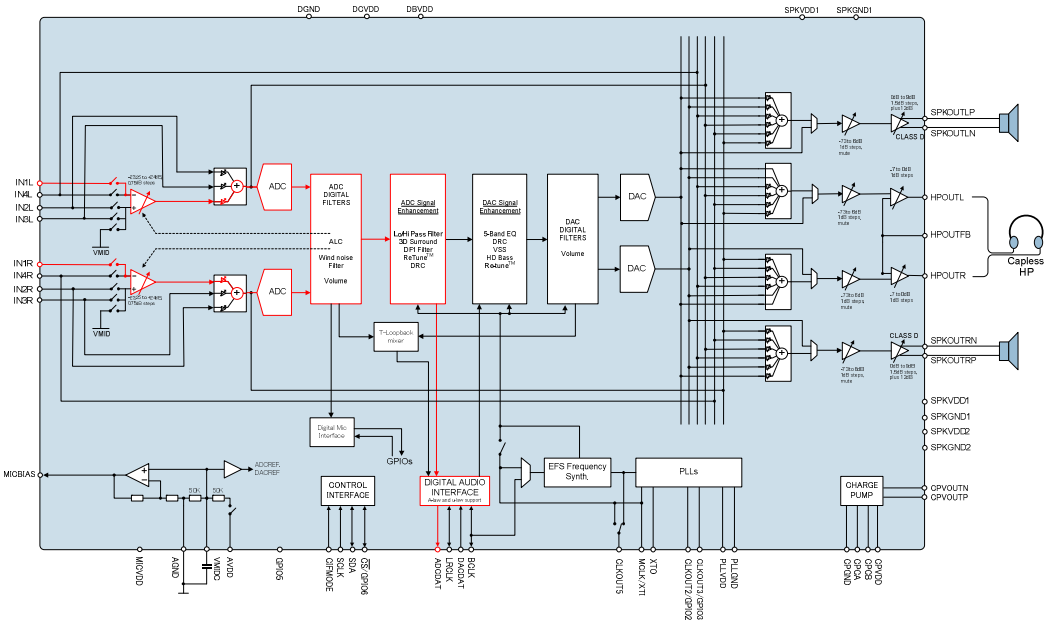


Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Red	Solid	2	DSP Anlr.THD+N Ampl A	Left	IN1 to ADC, left channel, C18 & R34 pop, driving on Headset jack
1	2	Blue	Solid	2	DSP Anlr.THD+N Ampl B	Left	IN1 to ADC, right channel, C18 & R34 pop, driving on mainboard phono (RED phono)

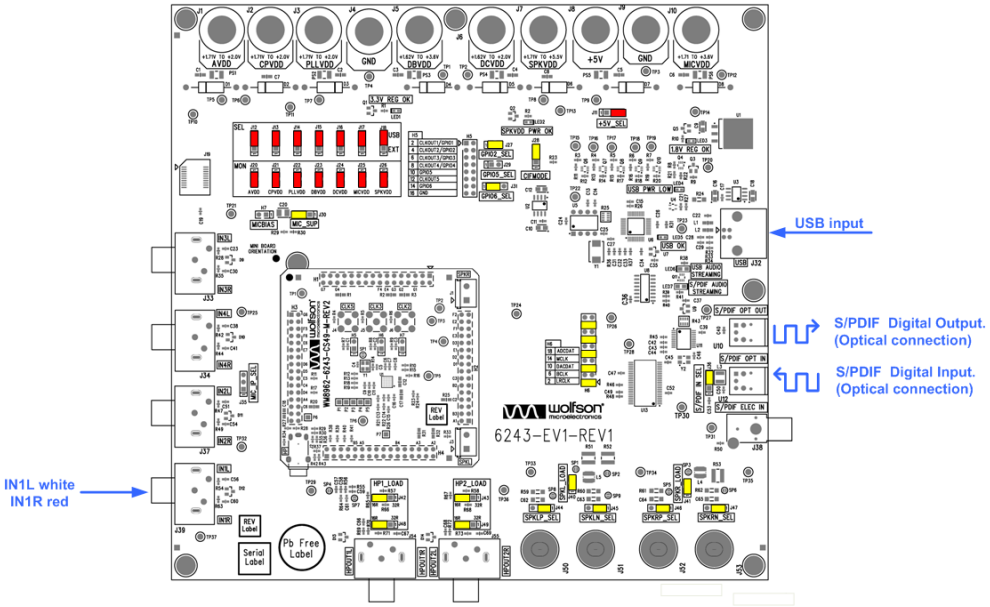
LINE IN1 TO ADC

The following section details board configuration for Line IN1 to ADC.

BLOCK DIAGRAM



BOARD CONFIGURATION



JUMPERS	JUMPER STATUS	DESCRIPTION
J11, J12, J13, J14, J15, J16, J17, J18	2 – 3	**USB power supply selected for all supplies**
J20, J21, J22, J23, J24, J25, J26	Links fitted	**Monitoring supplies**
J36	2 – 3	**S/PDIF_IN_SEL** Select the S/PDIF optical input.
H6	1 – 2 5 – 6 9 – 10 13 – 14 17 – 18	**AIF Interface** These links needed for connection to external clock source and Digital Dout derived from the S/PDIF interface.
J42,J48	2 – 3	**Headphones 1 Loads** Select 16R load
J43,J49	2 – 3	**Headphones 2 Loads** Select 16R load
J44 J40	1 – 2 Link fitted	**SPK_LP_SEL** Left channel positive analogue output on J50 with 8.2Ω load and no filter.
J45	1 – 2	**SPK_LN_SEL** Left channel negative analogue output on J51 with 8.2Ω load and no filter.
J46 J41	1 – 2 Link fitted	**SPK_RP_SEL** Right channel positive analogue output on J52 with 8.2Ω load and no filter.
J47	1 – 2	**SPK_RN_SEL** Right channel negative analogue output on J53 with 8.2Ω load and no filter.
J27	Link fitted	**GPIO2_SEL**
J28	2 – 3	**CIFMODE**
J29	Link not fitted	**GPIO5_SEL**
J31	1 – 2	**GPIO6_SEL**
J30	2 – 3	**MICSUP**
H7	1: MICBIAS 2: GND	**MICBIAS** Microphone bias voltage output on H7
J35	Link not fitted	**MIC_IP_SEL**

Table 5 Main Board 6243 Jumper Settings for IN1 to ADC using Optical S/PDIF

REGISTER SETTINGS

Register settings provided below are the minimum requirement to configure the desired audio path.

REG INDEX	DATA VALUE	COMMENT
Clocking configuration for 48kHz @ 256Fs		
0x0F - write	0x0000	Software Reset
0x81 - write	0x0001	Define OSC_ENA=0, PLL2_ENA=0, PLL3_ENA=0
0x7D - write	0x0048	Define CLKOUT2_DIV=0, CLKOUT5_DIV=0
0x7C - write	0x0000	Define CLKOUT3_SEL=00, CLKOUT5_SEL=0
0x08 - write	0x09C4	Set CLKREG_OVD=1 (clocking registers are controlled by the Control Interface), Disable system clock (SYSCLK_ENA = 0), Set system clock source to MCLK
0x38 - write	0x0506	Set MCLK_RATE to 256*Fs
0x1B - write	0x0010	Set SAMPLE_RATE to 48KHz
0x08 - write	0x09E4	Re-Enable system clock (SYSCLK_ENA=1), Ensure clocking registers are controlled normally via Control Interface (CLKREG_OVD=1)
0x1C - write	0x0018	Enable current bias circuits
0x19 - write	0x01C0	Bring up VMID quickly, enable master bias
Wait 4.5 ms		
IN1 to ADC audio path setup using Write Sequencer		
0x25 - write	0x0008	Set IN1L_TO_INPGAL=1
0x26 - write	0x0008	Set IN1R_TO_INPGAR=1
0x00 - write	0x011F	Unmute input left PGAs by setting INPGAL_MUTE=0, set 0dB volume
0x01 - write	0x011F	Unmute input right PGAs by setting INPGAR_MUTE=0, set 0dB volume
0x57 - write	0x0020	Enable write sequencer
0x5A - write	0x0092	Start write sequencer
Wait 150 ms for the Write Sequencer to finish		
0x5D - read	-	Read status of write sequencer to check that WSEQ CURRENT INDEX = 0000000 and WSEQ_BUSY = 0

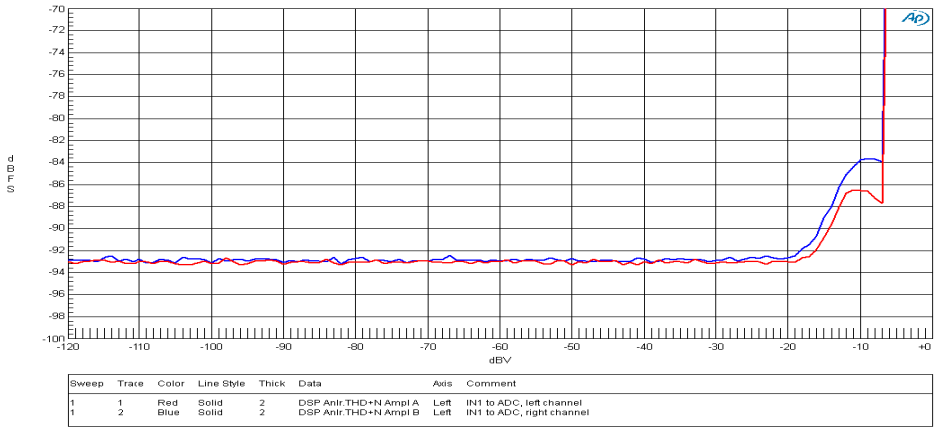
PERFORMANCE PLOT

AVDD = CPVDD = PLLVDD = DBVDD = DCVDD = 1.8V; SPKVDD = 5V; MICVDD = 2.5V

Sample Frequency = 48KHz

THD+N Amplitude (A-weighted)

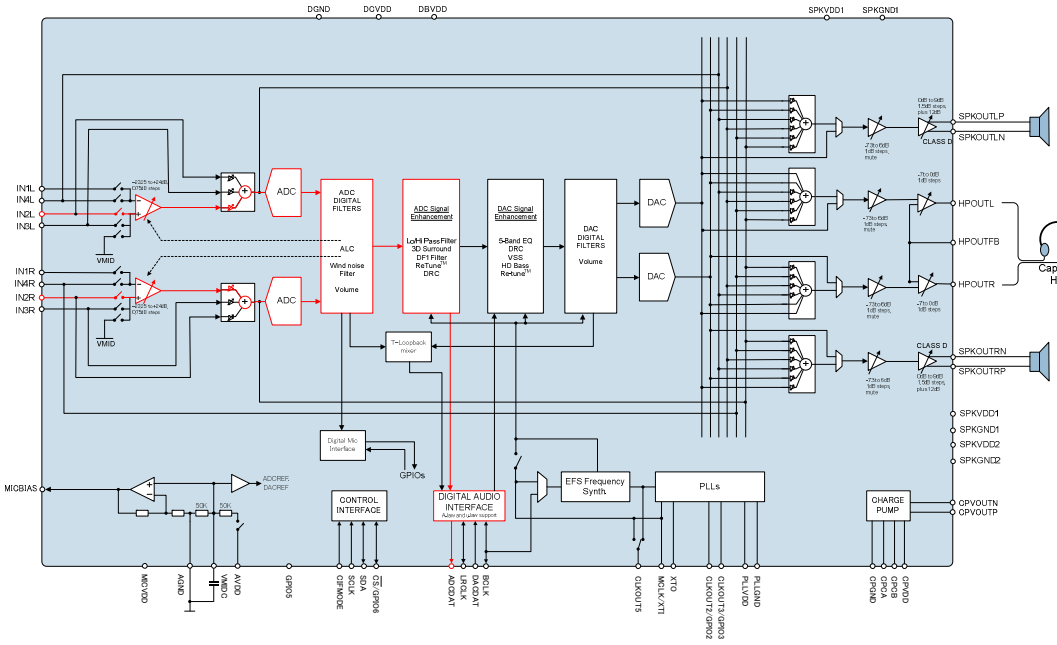
WM8962 ADC – THD+N v Amplitude – IN1 to ADC – Slave mode 256Fs – no Headset detect accessory being used and C18 and R34 unpopulated



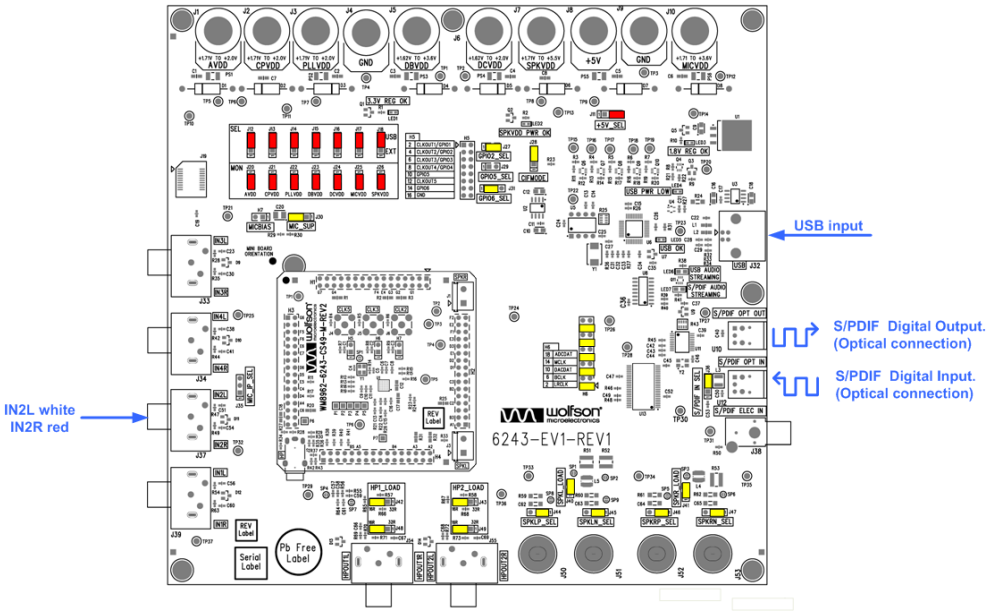
LINE IN2 TO ADC

The following section details board configuration for Line IN2 to ADC.

BLOCK DIAGRAM



BOARD CONFIGURATION



JUMPERS	JUMPER STATUS	DESCRIPTION
J11, J12, J13, J14, J15, J16, J17, J18	2 – 3	**USB power supply selected for all supplies**
J20, J21, J22, J23, J24, J25, J26	Links fitted	**Monitoring supplies**
J36	2 – 3	**S/PDIF_IN_SEL** Select the S/PDIF optical input.
H6	1 – 2 5 – 6 9 – 10 13 – 14 17 – 18	**AIF Interface** These links needed for connection to external clock source and Digital Dout derived from the S/PDIF interface.
J42,J48	2 – 3	**Headphones 1 Loads** Select 16R load
J43,J49	2 – 3	**Headphones 2 Loads** Select 16R load
J44 J40	1 – 2 Link fitted	**SPK_LP_SEL** Left channel positive analogue output on J50 with 8.2Ω load and no filter.
J45	1 – 2	**SPK_LN_SEL** Left channel negative analogue output on J51 with 8.2Ω load and no filter.
J46 J41	1 – 2 Link fitted	**SPK_RP_SEL** Right channel positive analogue output on J52 with 8.2Ω load and no filter.
J47	1 – 2	**SPK_RN_SEL** Right channel negative analogue output on J53 with 8.2Ω load and no filter.
J27	Link fitted	**GPIO2_SEL**
J28	2 – 3	**CIFMODE**
J29	Link not fitted	**GPIO5_SEL**
J31	1 – 2	**GPIO6_SEL**
J30	2 – 3	**MICSUP**
H7	1: MICBIAS 2: GND	**MICBIAS** Microphone bias voltage output on H7
J35	Link not fitted	**MIC_IP_SEL**

Table 6 Main Board 6243 Jumper Settings for IN2 to ADC using Optical S/PDIF

REGISTER SETTINGS

Register settings provided below are the minimum requirement to configure the desired audio path.

REG INDEX	DATA VALUE	COMMENT
Clocking configuration for 48kHz @ 256Fs		
0x0F - write	0x0000	Software Reset
0x81 - write	0x0001	Define OSC_ENA=0, PLL2_ENA=0, PLL3_ENA=0
0x7D - write	0x0048	Define CLKOUT2_DIV=0, CLKOUT5_DIV=0
0x7C - write	0x0000	Define CLKOUT3_SEL=00, CLKOUT5_SEL=0
0x08 - write	0x09C4	Set CLKREG_OVD=1 (clocking registers are controlled by the Control Interface), Disable system clock (SYSCLK_ENA = 0), Set system clock source to MCLK
0x38 - write	0x0506	Set MCLK_RATE to 256*Fs
0x1B - write	0x0010	Set SAMPLE_RATE to 48KHz
0x08 - write	0x09E4	Re-Enable system clock (SYSCLK_ENA=1), Ensure clocking registers are controlled normally via Control Interface (CLKREG_OVD=1)
0x1C - write	0x0018	Enable current bias circuits
0x19 - write	0x01C0	Bring up VMID quickly, enable master bias
Wait 4.5 ms		
IN2 to ADC audio path setup not using input PGA, using Write Sequencer		
0x1F - write	0x0003	Enable mixer stage
0x22 - write	0x0024	Route IN2 directly to mixer stage
0x57 - write	0x0020	Enable write sequencer
0x5A - write	0x0092	Start write sequencer
Wait 150 ms for the Write Sequencer to finish		
0x5D - read	-	Read status of write sequencer to check that WSEQ CURRENT INDEX = 0000000 and WSEQ_BUSY = 0

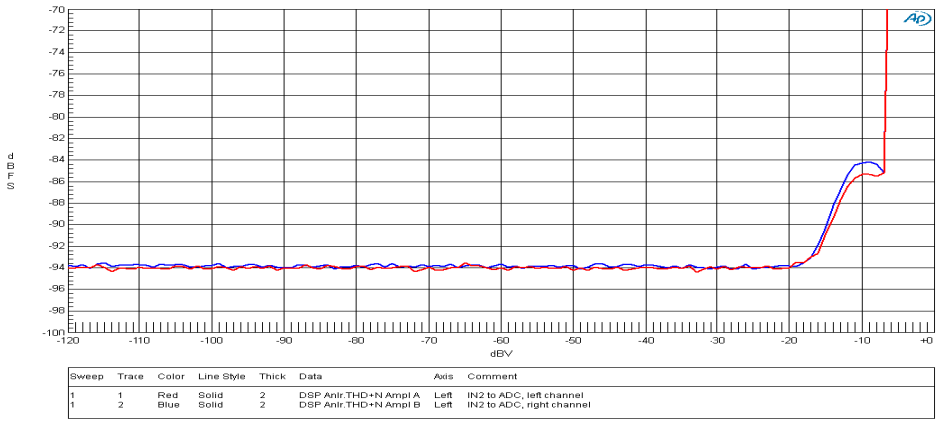
PERFORMANCE PLOT

AVDD = CPVDD = PLLVDD = DBVDD = DCVDD = 1.8V; SPKVDD = 5V; MICVDD = 2.5V

Sample Frequency = 48KHz

THD+N Amplitude (A-weighted)

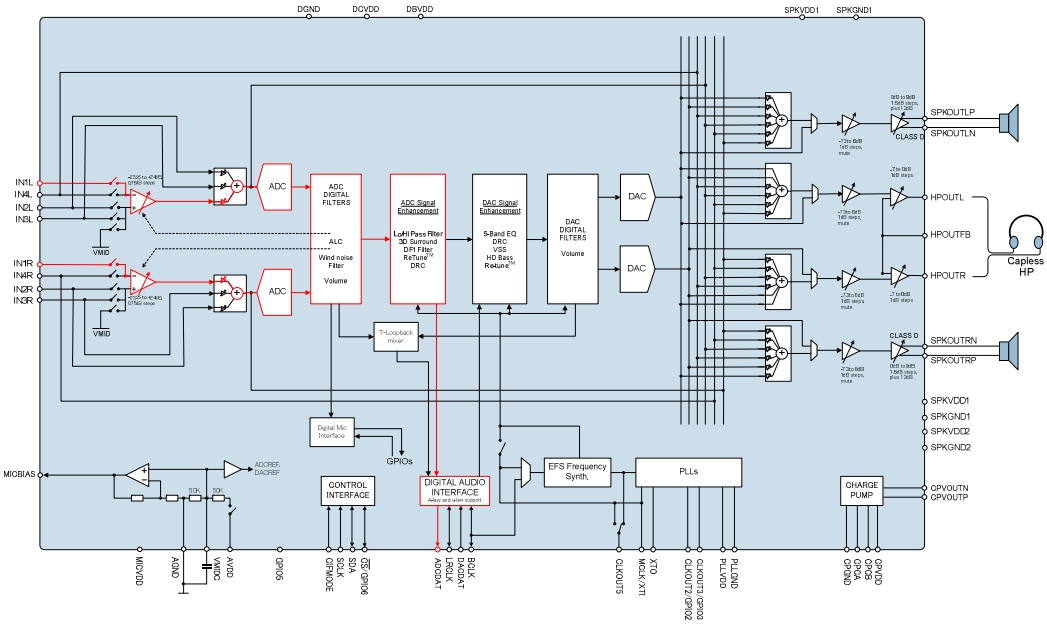
WM8962 ADC – THD+N v Amplitude – IN2 to ADC – Slave mode 256Fs – no Headset detect accessory being used and C18 and R34 unpopulated



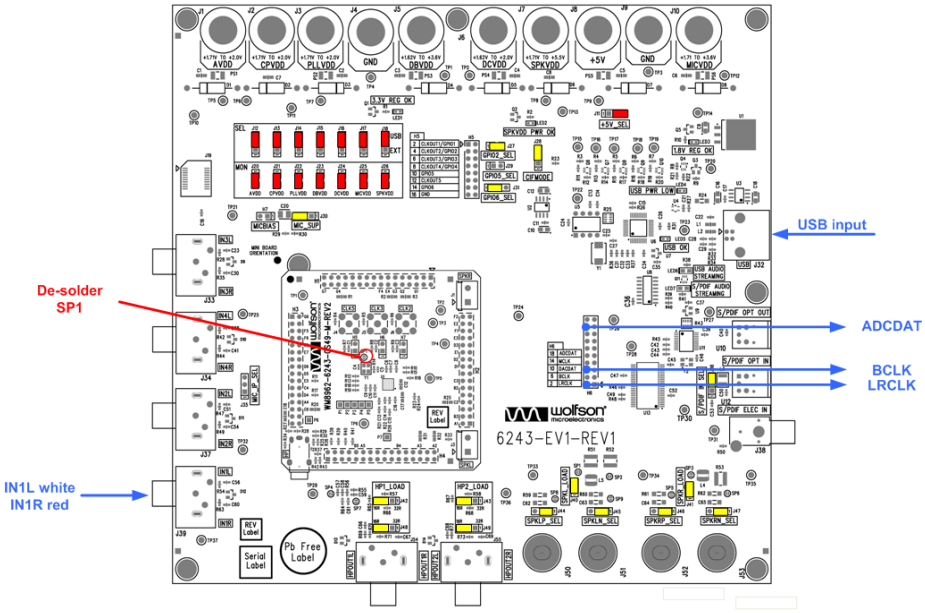
LINE IN1 TO ADC USING CRYSTAL OSCILLATOR

The following section details board configuration for Line IN1 to ADC using crystal oscillator.

BLOCK DIAGRAM



BOARD CONFIGURATION



JUMPERS	JUMPER STATUS	DESCRIPTION
J11, J12, J13, J14, J15, J16, J17, J18	2 – 3	**USB power supply selected for all supplies**
J20, J21, J22, J23, J24, J25, J26	Links fitted	**Monitoring supplies**
J36	2 – 3	**S/PDIF_IN_SEL** Select the S/PDIF optical input.
H6	2 : LRCLK 6 : BCLK 18 : ADCDAT	**AIF Interface** These pins are needed for connection to external equipment.
J42,J48	2 – 3	**Headphones 1 Loads** Select 16R load
J43,J49	2 – 3	**Headphones 2 Loads** Select 16R load
J44 J40	1 – 2 Link fitted	**SPK_LP_SEL** Left channel positive analogue output on J50 with 8.2Ω load and no filter.
J45	1 – 2	**SPK_LN_SEL** Left channel negative analogue output on J51 with 8.2Ω load and no filter.
J46 J41	1 – 2 Link fitted	**SPK_RP_SEL** Right channel positive analogue output on J52 with 8.2Ω load and no filter.
J47	1 – 2	**SPK_RN_SEL** Right channel negative analogue output on J53 with 8.2Ω load and no filter.
J27	Link fitted	**GPIO2_SEL**
J28	2 – 3	**CIFMODE**
J29	Link not fitted	**GPIO5_SEL**
J31	1 – 2	**GPIO6_SEL**
J30	2 – 3	**MICSUP**
H7	1 : MICBIAS 2 : GND	**MICBIAS** Microphone bias voltage output on H7
J35	Link not fitted	**MIC_IP_SEL**

Table 7 Main Board 6243 Jumper Settings for IN1 to ADC using the Crystal Oscillator and the Audio Interface in Master Mode

REGISTER SETTINGS

Register settings provided below are the minimum requirement to configure the desired audio path.

REG INDEX	DATA VALUE	COMMENT
Clocking configuration for 48kHz @ 512Fs, AIF master mode, using XTAL Oscillator and PLL3		
0x0F - write	0x0000	Software Reset
0x81 - write	0x0001	Define OSC_ENA =1, PLL2_ENA=0, PLL3_ENA=0
0x7D - write	0x0048	Define CLKOUT2_DIV=0, CLKOUT5_DIV=0
0x7C - write	0x0000	Define CLKOUT3_SEL=00, CLKOUT5_SEL=0
0x08 - write	0x09C4	Set CLKREG_OVD=1 (clocking registers are controlled by the Control Interface), Disable system clock (SYSCLK_ENA=0)
0x8C - write	0x0068	Configure PLL3 to generate 24.576MHz (custom N.K = 8.192)
0x8D - write	0x0031	
0x8E - write	0x0026	
0x8F - write	0x00EA	
0x7D - write	0x0043	Set PLL divider to /1 (PLL_SYSCLK_DIV=00)
0x81 - write	0x00F1	Enable PLL3
Wait 4 ms to allow PLL3 to complete startup		
0x38 - write	0x050A	Set MCLK_RATE (ratio MCLK/Fs) to 512
0x08 - write	0x0DE7	Set SYSCLK source to PLL3, re-enable system clock (SYSCLK_ENA=1) and set BCLK divide by 8 (BCLK_DIV=0111) to get the 3.072MHz, Ensure clocking registers are controlled normally via Control Interface (CLKREG_OVD=1)
0x07 - write	0x004A	Set AIF in master mode
0x0E - write	0x0040	Set AIF to 64 BCLK per LRCLK
0x1C - write	0x0018	Enable current bias circuits
0x19 - write	0x01C0	Bring up VMID quickly, enable master bias
Wait 4.5 ms		
IN1 to ADC audio path setup using Write Sequencer		
0x25 - write	0x0008	Set IN1L_TO_INPGAL=1
0x26 - write	0x0008	Set IN1R_TO_INPGAR=1
0x00 - write	0x011F	Unmute input left PGAs by setting INPGAL_MUTE=0, set 0dB volume
0x01 - write	0x011F	Unmute input right PGAs by setting INPGAR_MUTE=0, set 0dB volume
0x57 - write	0x0020	Enable write sequencer
0x5A - write	0x0092	Start write sequencer
Wait 150 ms for the Write Sequencer to finish		
0x5D - read	-	Read status of write sequencer to check that WSEQ CURRENT INDEX = 0000000 and WSEQ_BUSY = 0

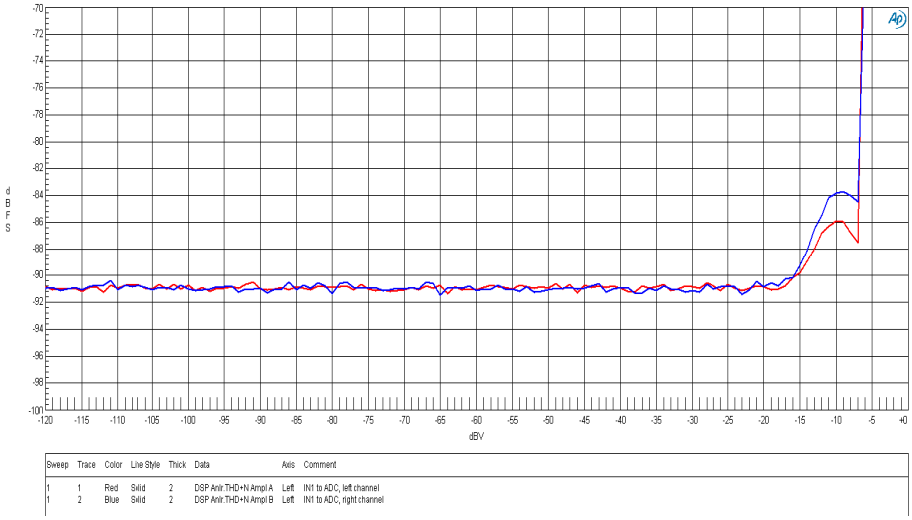
PERFORMANCE PLOT

AVDD = CPVDD = PLLVDD = DBVDD = DCVDD = 1.8V; SPKVDD = 5V; MICVDD = 2.5V

Sample Frequency = 48KHz

THD+N Amplitude (A-weighted)

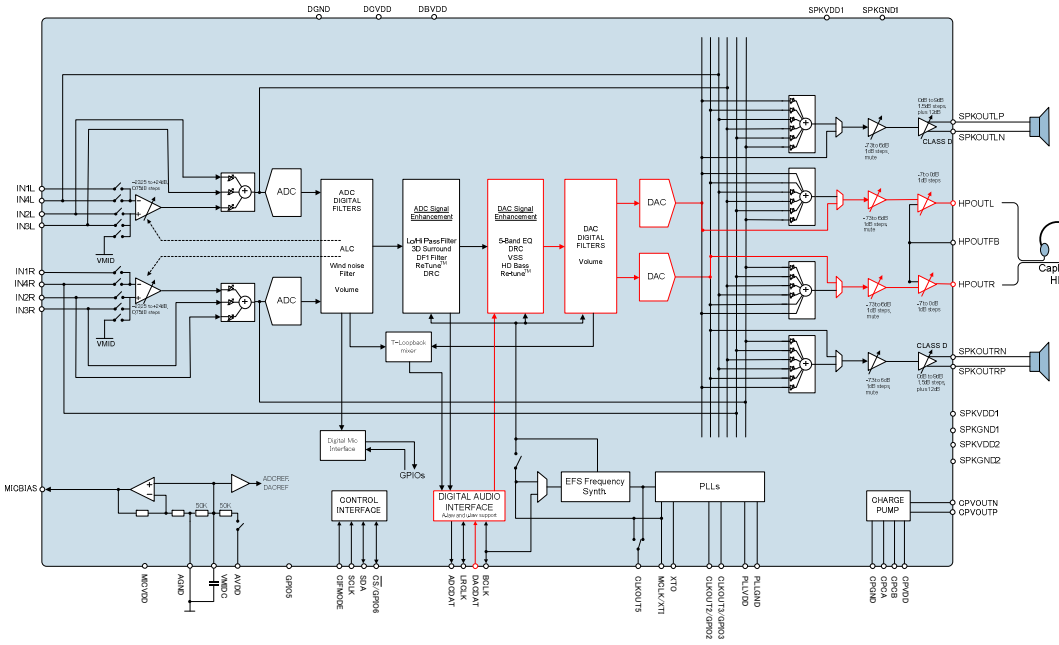
WM8962 ADC – THD+N v Amplitude – IN1 to ADC – Master mode 512Fs using crystal oscillator – no Headset detect accessory being used and C18 and R34 unpopulated



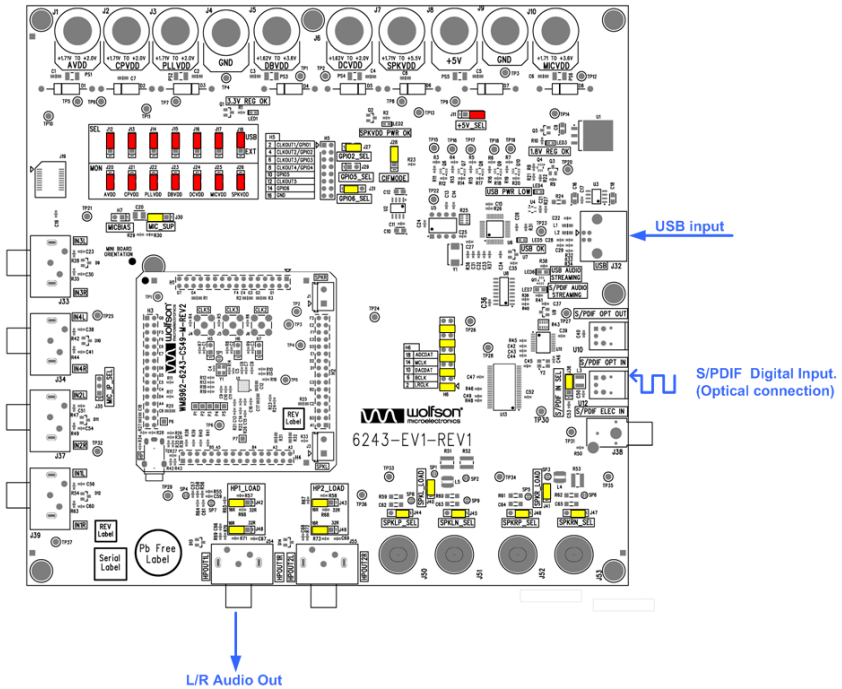
DAC TO HEADPHONES (16 OHM LOAD)

The following section details board configuration for DAC to Headphones.

BLOCK DIAGRAM



BOARD CONFIGURATION



JUMPERS	JUMPER STATUS	DESCRIPTION
J11, J12, J13, J14, J15, J16, J17, J18	2 – 3	**USB power supply selected for all supplies**
J20, J21, J22, J23, J24, J25, J26	Links fitted	**Monitoring supplies**
J36	2 – 3	**S/PDIF_IN_SEL** Select the S/PDIF optical input.
H6	1 – 2 5 – 6 9 – 10 13 – 14 17 – 18	**AIF Interface** These links needed for connection to external clock source and Digital Din derived from the S/PDIF interface.
J42,J48	2 – 3	**Headphones 1 Loads** Select 16R load
J43,J49	2 – 3	**Headphones 2 Loads** Select 16R load
J44 J40	1 – 2 Link fitted	**SPK_LP_SEL** Left channel positive analogue output on J50 with 8.2Ω load and no filter.
J45	1 – 2	**SPK_LN_SEL** Left channel negative analogue output on J51 with 8.2Ω load and no filter.
J46 J41	1 – 2 Link fitted	**SPK_RP_SEL** Right channel positive analogue output on J52 with 8.2Ω load and no filter.
J47	1 – 2	**SPK_RN_SEL** Right channel negative analogue output on J53 with 8.2Ω load and no filter.
J27	Link fitted	**GPIO2_SEL**
J28	2 – 3	**CIFMODE**
J29	Link not fitted	**GPIO5_SEL**
J31	1 – 2	**GPIO6_SEL**
J30	2 – 3	**MICSUP**
H7	1 : MICBIAS 2 : GND	**MICBIAS** Microphone bias voltage output on H7
J35	Link not fitted	**MIC_IP_SEL**

Table 8 Main Board 6243 Jumper Settings for DAC to Headphones using Optical S/PDIF

REGISTER SETTINGS

Register settings provided below are the minimum requirement to configure the desired audio path.

REG INDEX	DATA VALUE	COMMENT
Clocking configuration for 48kHz @ 512Fs from FLL fed with 256Fs		
0x0F - write	0x0000	Software Reset
0x81 - write	0x0001	Define OSC_ENA=0, PLL2_ENA=0, PLL3_ENA=0
0x7D - write	0x0048	Define CLKOUT2_DIV=0, CLKOUT5_DIV=0
0x7C - write	0x0000	Define CLKOUT3_SEL=00, CLKOUT5_SEL=0
0x08 - write	0x0BC4	Set CLKREG_OVD=1 (Clocking registers are controlled by the Control Interface), Disable system clock (SYSCLK_ENA=0), Set clock source from FLL
0x1C - write	0x0018	Enable current bias circuits
0x19 - write	0x01C0	Bring up VMID quickly, enable master bias
0x9C - write	0x0018	Set FLL_REFCLK_DIV to /1 and FLL_OUTDIV to /4
0x9D - write	0x0180	Set FLL_FRATIO to /1
0xA2 - write	0x0008	Set FLL_N to decimal 8
0x9B - write	0x0009	Set FLL clock source from MCLK, select FLL integer mode of operation, and enable FLL
Wait 2ms to allow FLL to complete startup		
0x38 - write	0x050A	Set MCLK_RATE to 512*Fs
0x1B - write	0x0010	Set SAMPLE_RATE to 48.000KHz
0x08 - write	0x0BE4	Re-Enable system clock
Wait 4.5 ms		
DAC to HP audio path setup, using Write Sequencer		
0x57 - write	0x0020	Enable write sequencer
0x5A - write	0x0080	Start write sequencer
Wait 250 ms for the Write Sequencer to finish		
0x5D - read	-	Read status of write sequencer to check that WSEQ CURRENT INDEX = 0000000 and WSEQ_BUSY = 0
Update Headphones PGA to 0dB		
0x02	0x00F9	Set HPOUT1 PGA volume to 0dB
0x03	0x01F9	

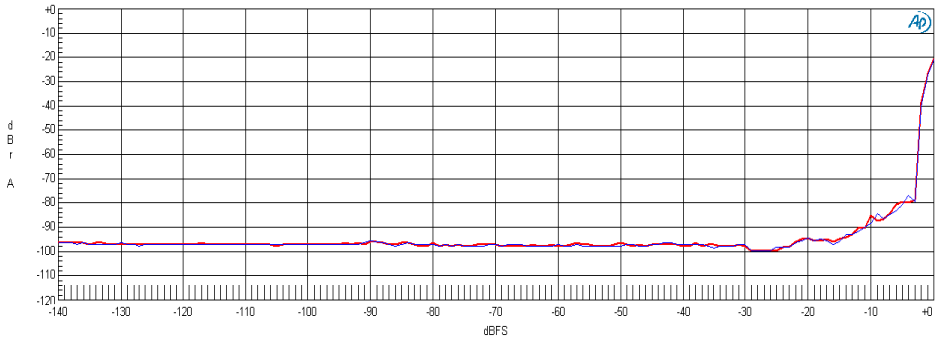
PERFORMANCE PLOT

AVDD = CPVDD = PLLVDD = DBVDD = DCVDD = 1.8V; SPKVDD = 5V; MICVDD = 2.5V

Sample Frequency = 48KHz

THD+N Amplitude (A-weighted) 16 ohms load

WM8962 ADC – THD+N v Amplitude – DAC to HP – Slave mode 512Fs from FLL 256Fs

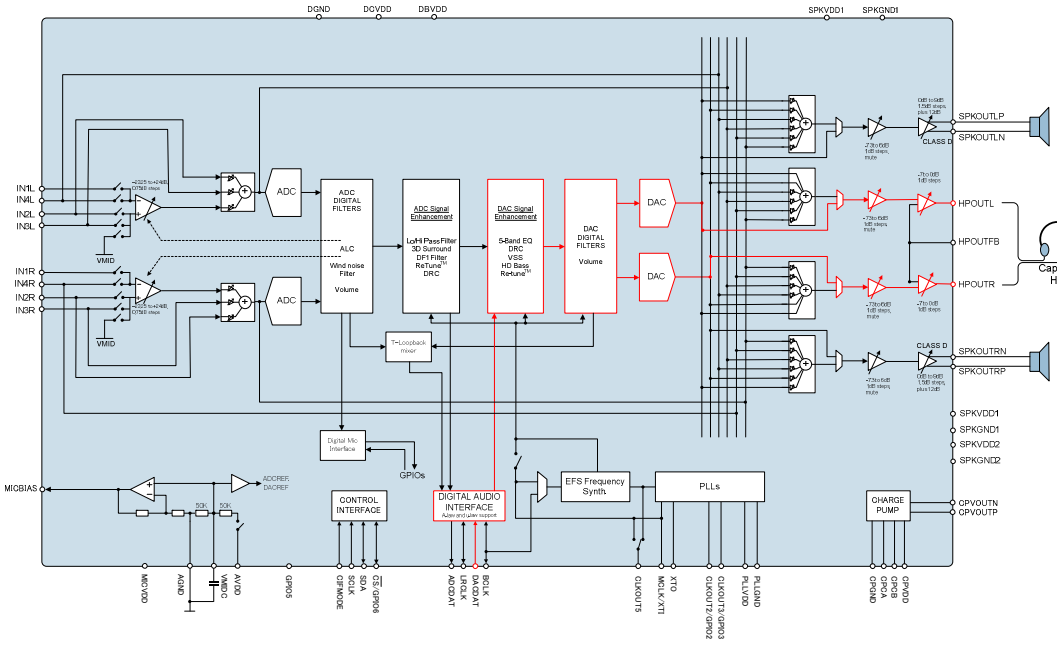


Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Red	Solid	2	Anlr:THD+N Ampl	Left	DAC to HP, left channel
1	2	Blue	Solid	1	Anlr:THD+N Ampl	Left	DAC to HP, right channel

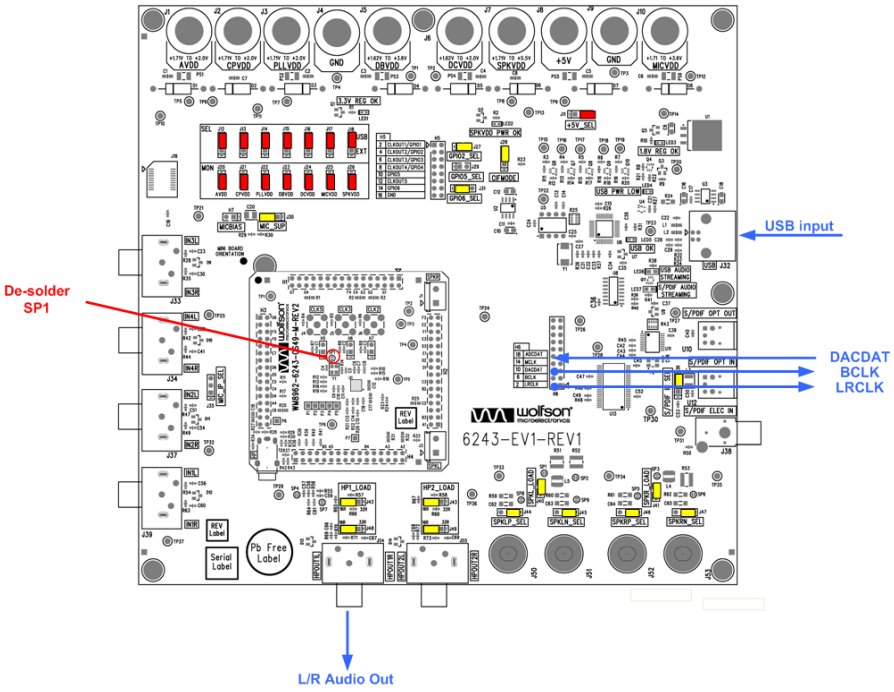
DAC TO HEADPHONES USING CRYSTAL OSCILLATOR (16 OHM LOAD)

The following section details board configuration for DAC to Headphones using crystal oscillator.

BLOCK DIAGRAM



BOARD CONFIGURATION



JUMPERS	JUMPER STATUS	DESCRIPTION
J11, J12, J13, J14, J15, J16, J17, J18	2 – 3	**USB power supply selected for all supplies**
J20, J21, J22, J23, J24, J25, J26	Links fitted	**Monitoring supplies**
J36	2 – 3	**S/PDIF_IN_SEL** Select the S/PDIF optical input.
H6	2 : LRCLK 6 : BCLK 10 : DACDAT	**AIF Interface** These pins are needed for connection to external equipment.
J42,J48	2 – 3	**Headphones 1 Loads** Select 16R load
J43,J49	2 – 3	**Headphones 2 Loads** Select 16R load
J44 J40	1 – 2 Link fitted	**SPK_LP_SEL** Left channel positive analogue output on J50 with 8.2Ω load and no filter.
J45	1 – 2	**SPK_LN_SEL** Left channel negative analogue output on J51 with 8.2Ω load and no filter.
J46 J41	1 – 2 Link fitted	**SPK_RP_SEL** Right channel positive analogue output on J52 with 8.2Ω load and no filter.
J47	1 – 2	**SPK_RN_SEL** Right channel negative analogue output on J53 with 8.2Ω load and no filter.
J27	Link fitted	**GPIO2_SEL**
J28	2 – 3	**CIFMODE**
J29	Link not fitted	**GPIO5_SEL**
J31	1 – 2	**GPIO6_SEL**
J30	2 – 3	**MICSUP**
H7	1 : MICBIAS 2 : GND	**MICBIAS** Microphone bias voltage output on H7
J35	Link not fitted	**MIC_IP_SEL**

Table 9 Main Board 6243 Jumper Settings for DAC to Headphones 2 using the Crystal Oscillator and the Audio Interface in Master Mode

REGISTER SETTINGS

Register settings provided below are the minimum requirement to configure the desired audio path.

REG INDEX	DATA VALUE	COMMENT
Clocking configuration for 48kHz @ 512Fs, AIF master mode, using XTAL Oscillator and PLL3		
0x0F - write	0x0000	Software Reset
0x81 - write	0x0001	Define OSC_ENA =1, PLL2_ENA=0, PLL3_ENA=0
0x7D - write	0x0048	Define CLKOUT2_DIV=0, CLKOUT5_DIV=0
0x7C - write	0x0000	Define CLKOUT3_SEL=00, CLKOUT5_SEL=0
0x08 - write	0x09C4	Set CLKREG_OVD=1 (clocking registers are controlled by the Control Interface), Disable system clock (SYSCLK_ENA=0)
0x8C - write	0x0068	Configure PLL3 to generate 24.576MHz (custom N.K = 8.192)
0x8D - write	0x0031	
0x8E - write	0x0026	
0x8F - write	0x00EA	
0x7D - write	0x0043	Set PLL divider to /1 (PLL_SYSCLK_DIV=00)
0x81 - write	0x00F1	Enable PLL3
Wait 4 ms to allow PLL3 to complete startup		
0x38 - write	0x050A	Set MCLK_RATE (ratio MCLK/Fs) to 512
0x08 - write	0x0DE7	Set SYSCLK source to PLL3, re-enable system clock (SYSCLK_ENA=1) and set BCLK divide by 8 (BCLK_DIV=0111) to get the 3.072MHz, Ensure clocking registers are controlled normally via Control Interface (CLKREG_OVD=1)
0x07 - write	0x004A	Set AIF in master mode
0x0E - write	0x0040	Set AIF to 64 BCLK per LRCLK
0x1C - write	0x0018	Enable current bias circuits
0x19 - write	0x01C0	Bring up VMID quickly, enable master bias
Wait 4.5 ms		
DAC to HP audio path setup, using Write Sequencer		
0x57 - write	0x0020	Enable write sequencer
0x5A - write	0x0080	Start write sequencer
Wait 250 ms for the Write Sequencer to finish		
0x5D - read	-	Read status of write sequencer to check that WSEQ CURRENT INDEX = 0000000 and WSEQ_BUSY = 0
Update Headphones PGA to 0dB		
0x02	0x00F9	Set HPOUT1 PGA volume to 0dB
0x03	0x01F9	

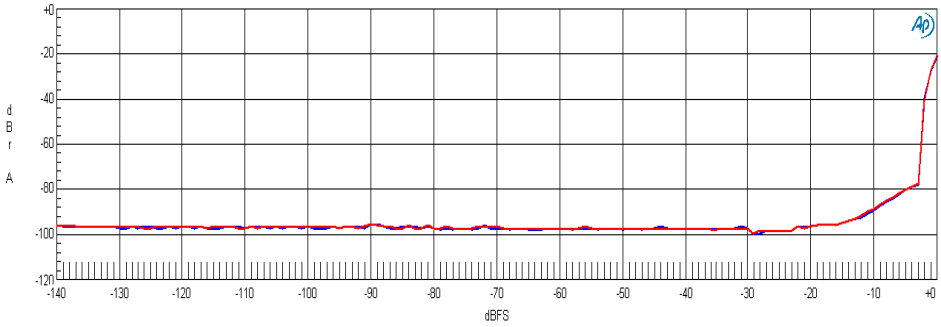
PERFORMANCE PLOT

AVDD = CPVDD = PLLVDD = DBVDD = DCVDD = 1.8V; SPKVDD = 5V; MICVDD = 2.5V

Sample Frequency = 48KHz

THD+N Amplitude (A-weighted) 16 ohms load

WM8962 ADC – THD+N v Amplitude – DAC to HP – Master mode 512Fs using crystal oscillator

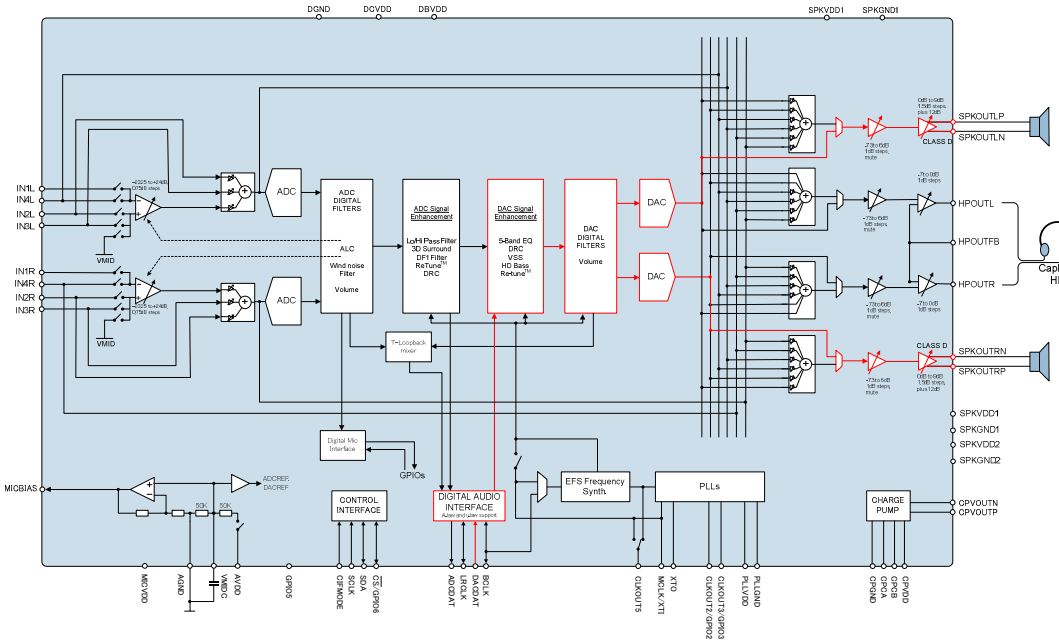


Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Red	Solid	2	Anlr.THD+N Ampl	Left	DAC to HP, left channel
1	2	Blue	Solid	2	Anlr.THD+N Ampl	Left	DAC to HP, right channel

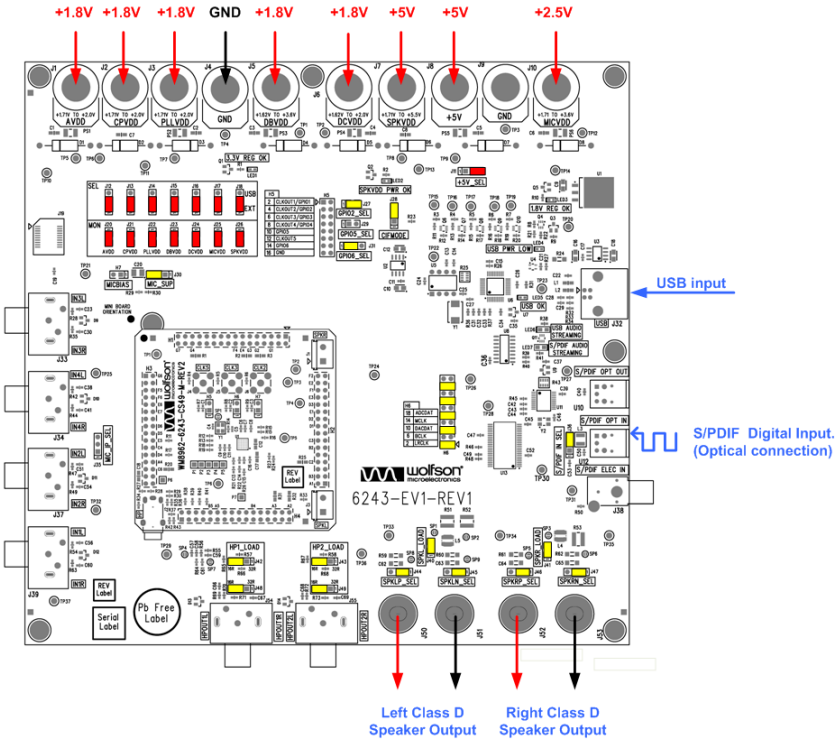
DAC TO SPEAKERS (8 OHM LOAD)

The following section details board configuration for DAC to Speakers.

BLOCK DIAGRAM



BOARD CONFIGURATION



JUMPERS	JUMPER STATUS	DESCRIPTION
J11, J12, J13, J14, J15, J16, J17, J18	2 – 3	**USB power supply selected for all supplies**
J20, J21, J22, J23, J24, J25, J26	Links fitted	**Monitoring supplies**
J36	2 – 3	**S/PDIF_IN_SEL** Select the S/PDIF optical input.
H6	1 – 2 5 – 6 9 – 10 13 – 14 17 – 18	**AIF Interface** These links needed for connection to external clock source and Digital Din derived from the S/PDIF interface.
J42,J48	2 – 3	**Headphones 1 Loads** Select 16R load
J43,J49	2 – 3	**Headphones 2 Loads** Select 16R load
J44 J40	1 – 2 Link fitted	**SPK_LP_SEL** Left channel positive analogue output on J50 with 8.2Ω load and no filter.
J45	1 – 2	**SPK_LN_SEL** Left channel negative analogue output on J51 with 8.2Ω load and no filter.
J46 J41	1 – 2 Link fitted	**SPK_RP_SEL** Right channel positive analogue output on J52 with 8.2Ω load and no filter.
J47	1 – 2	**SPK_RN_SEL** Right channel negative analogue output on J53 with 8.2Ω load and no filter.
J27	Link fitted	**GPIO2_SEL**
J28	2 – 3	**CIFMODE**
J29	Link not fitted	**GPIO5_SEL**
J31	1 – 2	**GPIO6_SEL**
J30	2 – 3	**MICSUP**
H7	1 : MICBIAS 2 : GND	**MICBIAS** Microphone bias voltage output on H7
J35	Link not fitted	**MIC_IP_SEL**

Table 10 Main Board 6243 Jumper Settings for DAC to Speakers using Optical S/PDIF

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REGISTER SETTINGS

Register settings provided below are the minimum requirement to configure the desired audio path.

REG INDEX	DATA VALUE	COMMENT
Clocking configuration for 48kHz @ 512Fs from FLL fed with 256Fs		
0x0F - write	0x0000	Software Reset
0x81 - write	0x0001	Define OSC_ENA=0, PLL2_ENA=0, PLL3_ENA=0
0x7D - write	0x0048	Define CLKOUT2_DIV=0, CLKOUT5_DIV=0
0x7C - write	0x0000	Define CLKOUT3_SEL=00, CLKOUT5_SEL=0
0x08 - write	0x0BC4	Set CLKREG_OVD=1 (Clocking registers are controlled by the Control Interface), Disable system clock (SYSCLK_ENA=0), Set clock source from FLL
0x1C - write	0x0018	Enable current bias circuits
0x19 - write	0x01C0	Bring up VMID quickly, enable master bias
0x9C - write	0x0018	Set FLL_REFCLK_DIV to /1 and FLL_OUTDIV to /4
0x9D - write	0x0180	Set FLL_FRATIO to /1
0xA2 - write	0x0008	Set FLL_N to decimal 8
0x9B - write	0x0009	Set FLL clock source from MCLK, select FLL integer mode of operation, and enable FLL
Wait 2ms to allow FLL to complete startup		
0x38 - write	0x050A	Set MCLK_RATE to 512*Fs
0x1B - write	0x0010	Set SAMPLE_RATE to 48.000KHz
0x08 - write	0x0BE4	Re-Enable system clock
Wait 4.5 ms		
DAC to SPK audio path setup		
0x1A - write	0x0198	Enable the DACs and Speaker PGAs
0x61- write	0x003F	Isolate dependency on HPOUT1 PGAs
0x28 - write	0x0079	Configure the Speaker PGAs for 0dB volume
0x29 - write	0x0179	
0x33 - write	0x0000	Configure ACGAIN for 0dB volume
0x31 - write	0x00C0	Enable the Speaker Outputs
0x06 - write	0x2008	Do a DAC soft unmute
0x05 - write	0x0010	

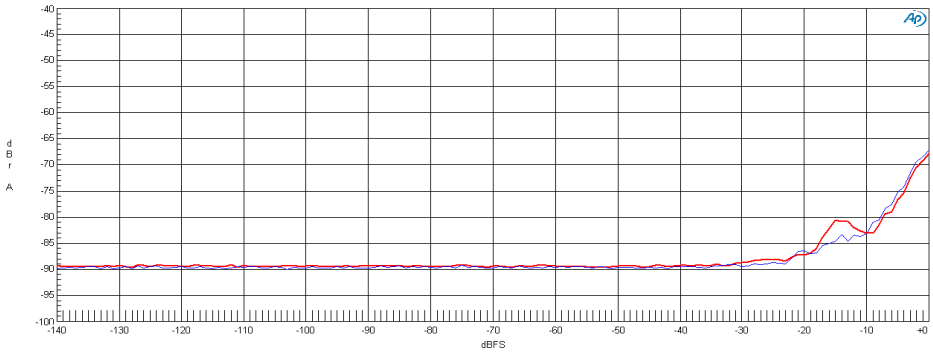
PERFORMANCE PLOT

AVDD = CPVDD = PLLVDD = DBVDD = DCVDD = 1.8V; SPKVDD = 5V; MICVDD = 2.5V

Sample Frequency = 48KHz

THD+N Amplitude (A-weighted) 8 ohms load

WM8962 ADC – THD+N v Amplitude – DAC to HP – Slave mode 512Fs from FLL 256Fs



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Red	Solid	2	Anlr.THD+N Ampl	Left	DAC to SPK, left channel
1	2	Blue	Solid	1	Anlr.THD+N Ampl	Left	DAC to SPK, right channel

GENERAL HARDWARE SETUP INFORMATION

BOARD POWER SUPPLIES

The 6243-EV1-REV1 customer evaluation board power supplies can be supplied using one of two sources:

- Individual external power supplies
- Derived from the USB connection or an external +5V.

The evaluation board can be powered either from the 4mm power lead receptacles (see Table 12) or from the USB/+5V host. Selection of using external power supplies or USB/+5V powered is made using the links shown in Table 1.

REF-DES	LINK STATUS	DESCRIPTION
J11 (+5V_SEL)		**+5V Power Source Select**
	1 - 2	+5V 4mm power jack receptacle selected
	2 - 3	USB power source selected (see note 1) [default setting]
J12 (AVDD_SEL)		**AVDD Power Source Select**
	1 - 2	AVDD 4mm power jack receptacle selected
	2 - 3	1.8v regulator, derived from either USB power source or 5V power selected (depending on J11) [default setting]
J13 (CPVDD_SEL)		**CPVDD Power Source Select**
	1 - 2	CPVDD 4mm power jack receptacle selected
	2 - 3	1.8v regulator, derived from either USB power source or 5V power selected (depending on J11) [default setting]
J14 (PLLVDD_SEL)		**PLLVDD Power Source Select**
	1 - 2	PLLVDD 4mm power jack receptacle selected
	2 - 3	1.8v regulator, derived from either USB power source or 5V power selected (depending on J11) [default setting]
J15 (DBVDD_SEL)		**DBVDD Power Source Select**
	1 - 2	DBVDD 4mm power jack receptacle selected
	2 - 3	1.8v regulator, derived from either USB power source or 5V power selected (depending on J11) [default setting]
J16 (DCVDD_SEL)		**DCVDD Power Source Select**
	1 - 2	DCVDD 4mm power jack receptacle selected
	2 - 3	1.8v regulator, derived from either USB power source or 5V power selected (depending on J11) [default setting]
J17 (MICVDD_SEL)		**MICVDD Power Source Select**
	1 - 2	MIC_VDD 4mm power jack receptacle selected
	2 - 3	1.8v regulator, derived from either USB power source or 5V power selected (depending on J11) [default setting]
J18 (SPKVDD_SEL)		**SPKVDD1 and SPK2VDD Power Source Select**
	1 - 2	SPKVDD 4mm power jack receptacle selected
	2 - 3	USB power source (not recommended - see note 1) or 5V power source selected (depending on J11) [default setting]

Table 11 Power Supply Source Select

Note:

1. USB nominal supply voltage is 5V, however this will reduce with several USB devices powered off the PC, or when a hub is used. In particular, under extreme load conditions (such as using the speaker output at full power), the voltage may drop to around 4V or lower. **Hence the USB power source is not recommended for evaluating the speaker outputs.**

If the board is being powered using external power supplies, using appropriate power leads with 4mm connectors, supplies can be connected as described in Table 12.

REF-DES	SOCKET NAME	SUPPLY
J1	AVDD	+1.7V to +2.0V
J2	CPVDD	+1.7V to +2.0V
J3	PLLVDD	+1.7V to +2.0V
J4	GND	0V
J5	DBVDD	+1.62V to +2.0V
J6	DCVDD	+1.62V to +2.0V
J7	SPKVDD	+1.7V to 5.5V
J8	+5V	+5V
J9	GND	0V
J10	MICVDD	+1.7V to 3.6V

Table 12 External Power Supply Connections

Note: Refer to the datasheet for limitations on individual supply voltages.

Important: Exceeding the recommended maximum voltage can damage EVB components. Under voltage may cause improper operation of some or all of the EVB components.

POWER SUPPLY CURRENT MONITORING

MEASURING CURRENT

The WM8962 current drawn by the WM8962 from each power supply on the customer evaluation can be measured at the red jumper links. To measure current, the red jumper, shown in Table 13, should be replaced by a current measuring meter.

REF-DES	LINK NAME	SUPPLY CURRENT
J20	AVDD	AVDD
J21	CPVDD	CPVDD
J22	PLLVDD	PLLVDD
J23	DBVDD	DVDD
J24	DCVDD	N/A
J25	MICVDD	MICVDD
J26	SPKVDD	SPKVDD (see note)

Table 13 Power Supply Current Measuring Links

Note: There is a quiescent current drawn by the test equipment filter as described in the following section.

TEST EQUIPMENT FILTER

The speaker output test equipment filter as shown in figure 6 is populated for best performance when measuring the speaker output. There is a quiescent current through SPKVDD associated with this filter. Removing the Test Equipment Filters by removing the solder bridge across SP8, SP9, SP5, SP6 as shown in Figure 6 will reduce the quiescent current through SPKVDD, hence is the best solution for current measurements.

Removing this filter may affect speaker audio performance when using measurement equipment, due to the class D switching frequency. A class D measurement filter such as the Audio Precision AUX0025 (see http://www.ap.com) is effective at filtering out such frequencies however note that AUX0025 also has a quiescent current associated with it. Using such a class D measurement filter or leaving the components on the PCB is the best solution for performance measurement.

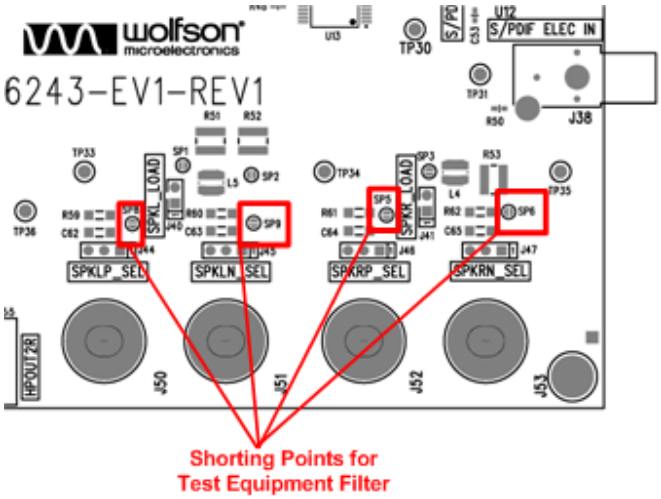


Figure 6 6243-EV1-REV1 Speaker Output Test Equipment Filter

S/PDIF INPUTS

The 6243-EV1-REV1 evaluation board supports both electrical and optical input of the S/PDIF stream. This signal may be input via a standard phono connector J38 or via the optical receivers U12. The selection is made using header J36. Refer to Table 14 S/PDIF Input Connections for details.

REF-DES	LINK STATUS	DESCRIPTION
J36		**S/PDIF Input Source Select**
	1 - 2	Electrical input selected [default setting]
	2 - 3	Optical input selected

Table 14 S/PDIF Input Connections

DIGITAL INPUTS AND CLOCK INPUTS

The 6243-EV1-REV1 evaluation board allows AIF data and clocks to be applied through a 20 pin header (H6) or through the S/PDIF interface. The following Table 15 shows the connections necessary. When H5 is not being used, the links should be put in place as described in this table.

REF-DES	PIN	DESCRIPTION
H6	1-2	AIF LRCLK input. Requires link between pins 1-2 when H6 not connected to external source.
	5-6	AIF BCLK input. Requires link between pins 5-6 when H6 not connected to external source.
	9-10	AIF Digital Input Data. Requires link between pins 9-10 when H6 not connected to external source.
	13-14	AIF MCLK input. Requires link between pins 13-14 when H6 not connected to external source.
	17-18	AIF Digital output Data. Requires link between pins 17-18 when H6 not connected to external source.

Table 15 AIF Input via Header H6

ANALOGUE INPUTS

The 6243-EV1-REV1 evaluation board is equipped to connect either a line level signal or a microphone input signal.

LINE INPUT

A line level input signal can be connected to the 6243-EV1-REV1 via the dual Phono connector J39 for IN1 or J34 for IN4.

MICROPHONE INPUT

A single-ended microphone can be connected to the input connector IN1 or IN4. For microphone biasing connections details see Table 16.

REF-DES	PIN	DESCRIPTION
H7		**MICP_SUP**
	1	MICBIAS
	2	GND

Table 16 Microphone Bias

MICROPHONE DAUGHTER CARD

A Wolfson Silicon microphone daughter card can be fitted facing outwards to connector J19. For microphone biasing connections details see Table 17.

REF-DES	PIN	DESCRIPTION
J35	1 - 2	**MICP_IP_SEL** Route Silicon microphone analogue output to IN1

Table 17 Wolfson Silicon Microphone Analogue Output Routing

ANALOGUE OUTPUTS

HEADPHONE OUTPUT

The 6243-EV1-REV1 evaluation board allows monitoring of the WM8962 analogue headphone outputs directly from the WM8962 device outputs. The WM8962 headphone outputs are available on the phono socket J54 and J55. The headphone output load can be selected between 16Ω and 32Ω using the headers J42 and J48 for Headphone 1 and headers J43 and J49 for Headphone 2. The selection of output load is shown in following table.

REF-DES	LINK STATUS	DESCRIPTION
J42 or J43		**HP_L_LOAD**
	1 - 2	Left channel headphone output load = 32Ω
	2 - 3	Left channel headphone output load = 16Ω
J48 and J49		**HP_R_LOAD**
	1 - 2	Right channel headphone output load = 32Ω
	2 - 3	Right channel headphone output load = 16Ω

Table 18 Headphone Output Load Selection

CLASS D SPEAKER OUTPUTS

The 6243-EV1-REV1 evaluation board allows speaker connection using the gold coloured binding posts. The evaluation board also offers the capability of providing a test load to the WM8962 Class D speaker drivers as well as allowing the connection of test equipment (AP2) filter.

The Class D speaker connections, load selection and test equipment filter selection are shown in Table 19, Table 20 and Table 21.

REF-DES	DESCRIPTION
J50	**SPK_LP** Class D left speaker positive connection output
J51	**SPK_LN** Class D left speaker negative connection output
J52	**SPK_RP** Class D right speaker positive connection output
J53	**SPK_RN** Class D right speaker negative connection output

Table 19 Class D Speaker Output Connections

REF-DES	LINK STATUS	DESCRIPTION
J40		**SPK_L_LOAD**
	Link in place	**8**.2Ω load presented to Class D left speaker output
	No link in place	No load presented to Class D left speaker output
J41		**SPK_R_LOAD**
	Link in place	**8**.2Ω load presented to Class D right speaker output
	No link in place	No load presented to Class D right speaker output

Table 20 Class D Speaker Output Load Connections

REF-DES	LINK STATUS	DESCRIPTION
J44		**SPK_LP_SEL**
	1-2	Low Pass Filter **not** connected to Class D left speaker +ve output
	2-3	Low Pass Filter connected to Class D left speaker +ve output
J45		**SPK_LN_SEL**
	1-2	Low Pass Filter **not** connected to Class D left speaker -ve output
	2-3	Low Pass Filter connected to Class D left speaker -ve output
J46		**SPK_RP_SEL**
	1-2	Low Pass Filter **not** connected to Class D right speaker +ve output
	2-3	Low Pass Filter connected to Class D right speaker +ve output
J47		
	1-2	Low Pass Filter **not** connected to Class D right speaker -ve output
	2-3	Low Pass Filter connected to Class D right speaker -ve output

Table 21 Class D Speaker Output Test Equipment Filter Connections

USB CONTROL

The 6243-EV1-REV1 evaluation board is equipped with a USB interface MCU which allows interconnection with a PC in conjunction with the 6243-EV1-REV1 evaluation software.

SOLDER PADS

Both the MAIN and mini boards have solder pads connections. These are connections which when bridged, route signals to different connectors. The following table gives details on when the solder pad bridge should be connected.

BOARD	REF-DES	SP STATUS	DESCRIPTION
mini	SP1	Bridged	Master clock is provided externally through the Audio Interface
mini	SP1	Not Bridged	WM8962 is clocked from the internal crystal oscillator
MAIN	SP1 SP3	Not Bridged Not Bridged	Left speaker output load includes a 10uH inductor. Right speaker output load includes a 10uH inductor
MAIN	SP1 SP3	Bridged Bridged	Left speaker output load is resistive only. Right speaker output load is resistive only.
MAIN	SP2	Bridged	This configuration is used when Left and Right speakers drivers are tied together to drive 2W into 4 ohms mode.
MAIN	SP2	Not Bridged	Left and Right speaker output load is 8 ohms
MAIN	SP8 SP9 SP5 SP6	Bridged Bridged Bridged Bridged	Test Equipment Filter connected across the Class D outputs
MAIN	SP8 SP9 SP5 SP6	Not Bridged Not Bridged Not Bridged Not Bridged	Test Equipment Filter is not connected across the Class D outputs
MAIN	SP4 SP7	Bridged Bridged	Retune™ Demo Filter connected across WM8962 Headphone 1 Left and J48 phono connector Headphone 1 Left. Please also remove 0R link R69. Retune Demo Filter introduces a non ideality in the frequency response of the Left Headphone 1. This artificially introduced non-ideality can be neutralized by running the WM8962 ReTune™ feature, hence demonstrating the ReTune™ capability of flattening out the frequency response of any Headphones.
MAIN	SP4 SP7	Not Bridged Not Bridged	Retune™ Demo Filter not in use. Please also ensure that R69 is populated with a 0R link.

Table 22 Main and mini Board Solder Pad (SP) Connections

LED INDICATORS

The 6243-EV1-REV1 evaluation board has a number of LEDs.

Their function is described in Table 23.

LED	REF_DES	DESCRIPTION	
		LED OFF	LED ON
LED1	3.3V REG OK	+3.3V Voltage regulator not operational.	+3.3V Voltage regulator OK
LED2	SPKVDD PWR OK	No Class D speaker voltage available	Class D speaker voltage is OK
LED3	1.8V REG OK	+1.8V Voltage regulator not operational.	+1.8V Voltage regulator OK
LED4	USB PWR LOW	USB Power OK. **Note**: this does not guarantee that there is sufficient power to drive speaker outputs within specified distortion levels – an external supply is recommended for SPKVDD during speaker testing.	RED = USB Power is low.
LED5	USB OK	USB Interface non-operational	USB Interface operational
LED6	USB AUDIO STREAMING	Audio is being streamed over S/PDIF	Audio is being streamed over USB or no S/PDIF input is present
LED7	S/PDIF AUDIO STREAMING	Audio is being streamed over USB or no S/PDIF input is present	Audio is being streamed over S/PDIF

Table 23 LED Descriptions

TECHNICAL SUPPORT

If you require more information or require technical support, please contact the nearest Wolfson Microelectronics regional office:
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ADDRESS:

Wolfson Microelectronics plc

Westfield House

26 Westfield Road

Edinburgh

EH11 2QB

United Kingdom

Tel :: +44 (0)131 272 7000

Fax :: +44 (0)131 272 7001

E-mail :: apps@wolfsonmicro.com