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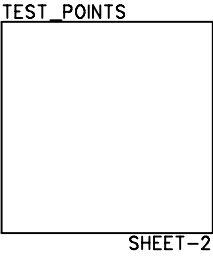
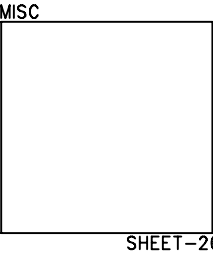
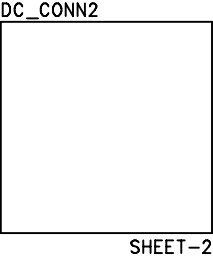
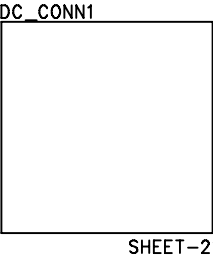
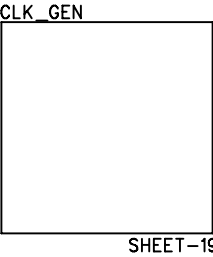
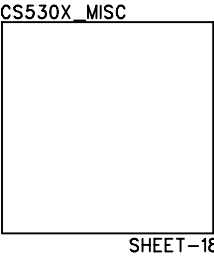
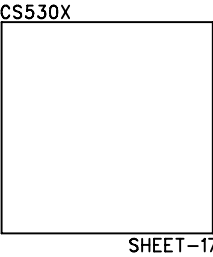
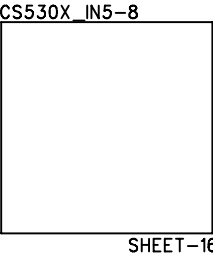
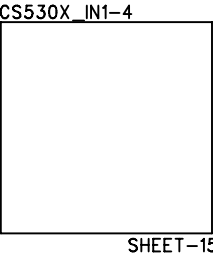
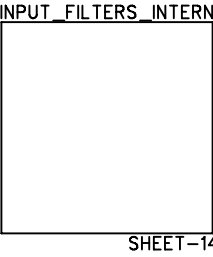
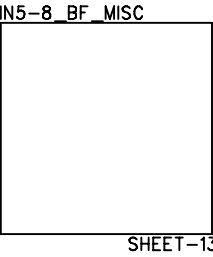
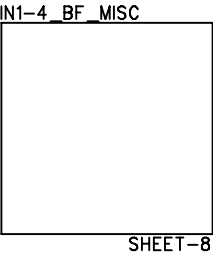
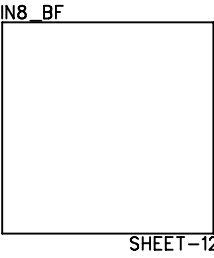
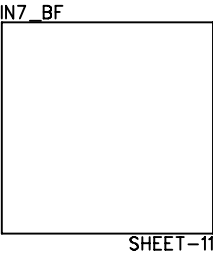
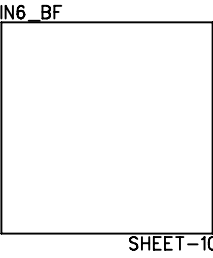
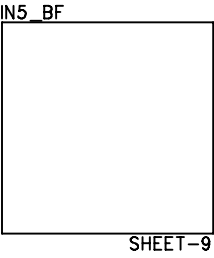
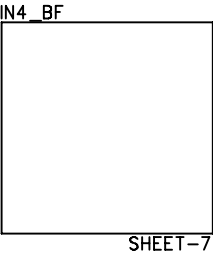
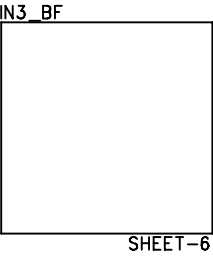
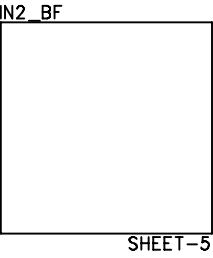
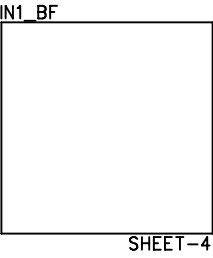
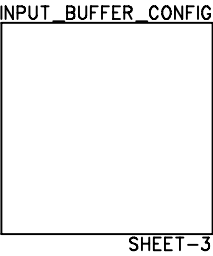
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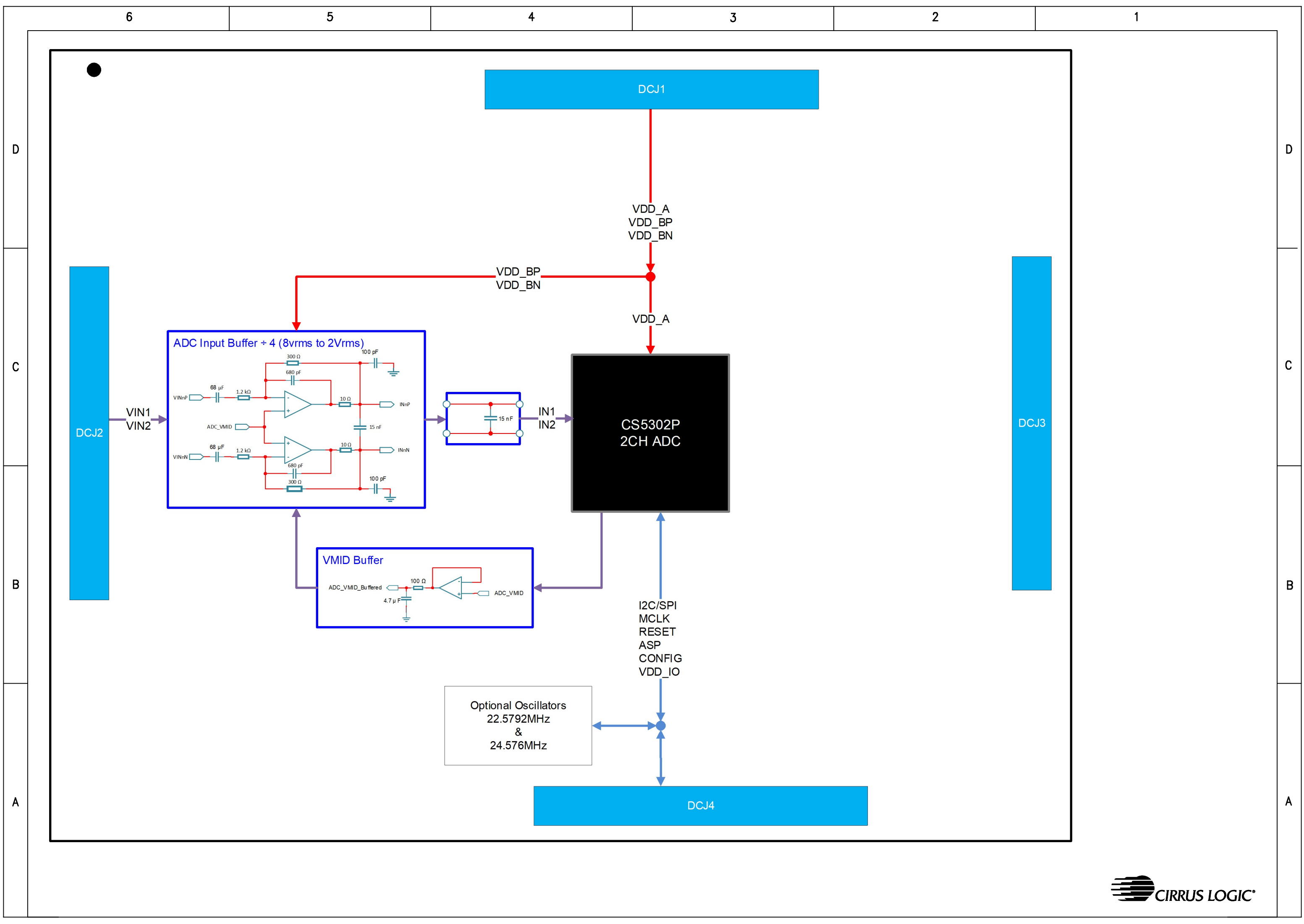
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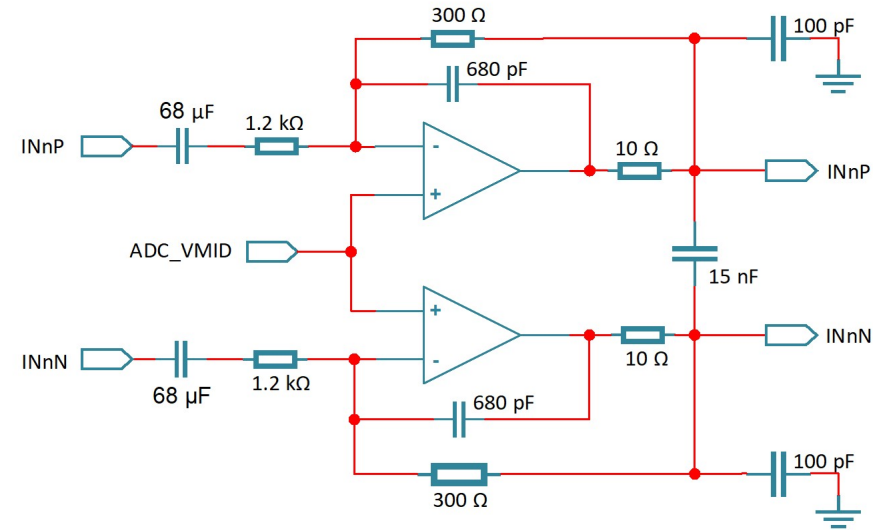




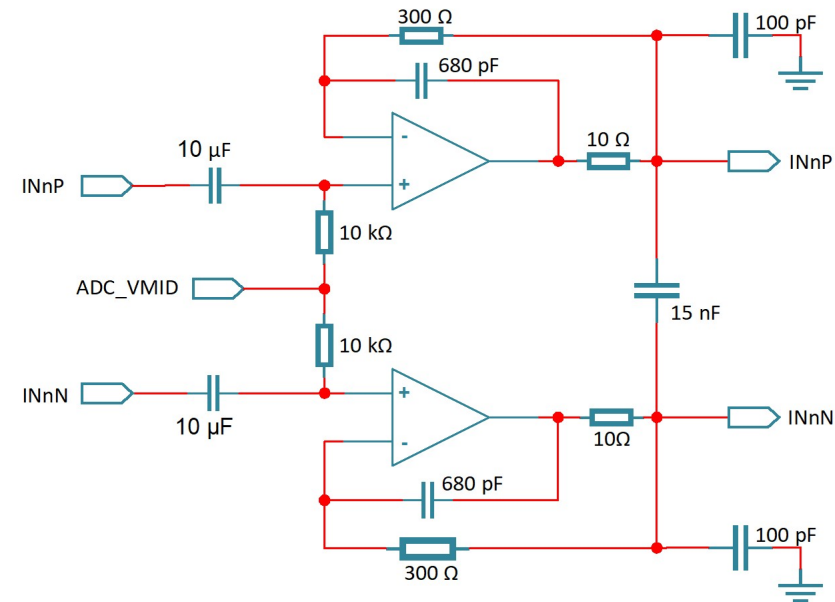
Input Buffer/Filter Options

Differential Input Circuits

Inverting

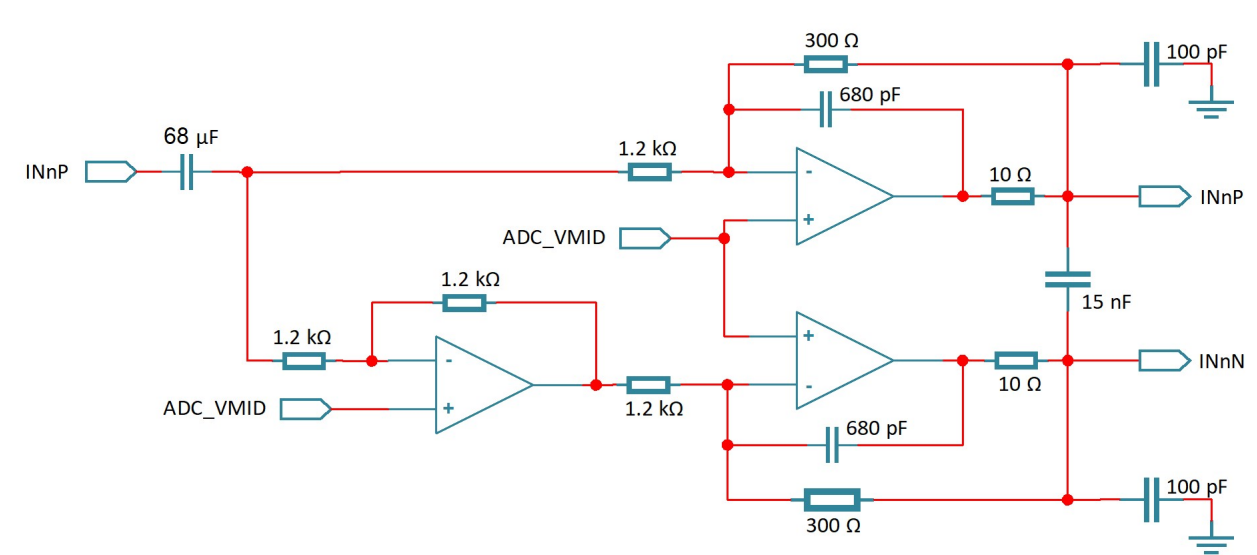


Non-Inverting (ADC VMID must be buffered in this use case)

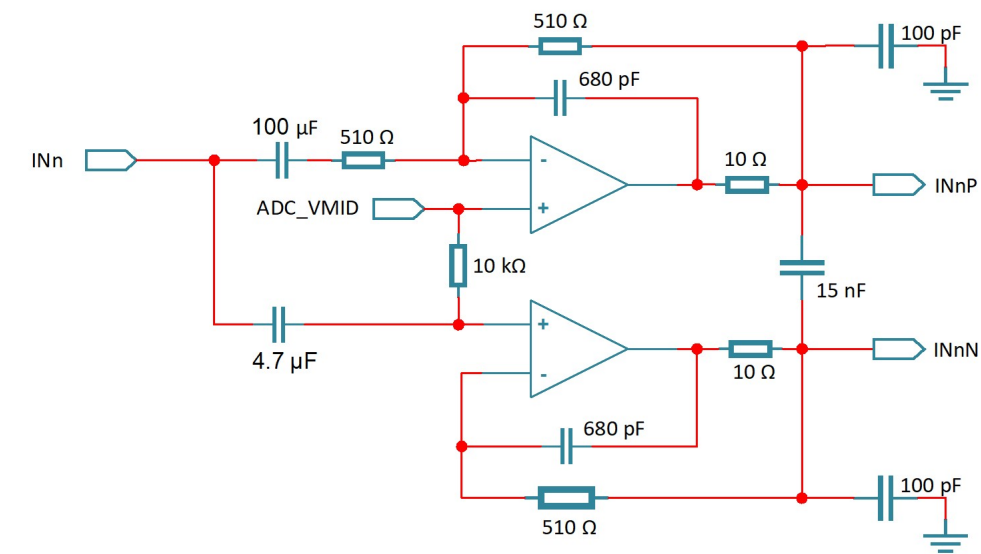


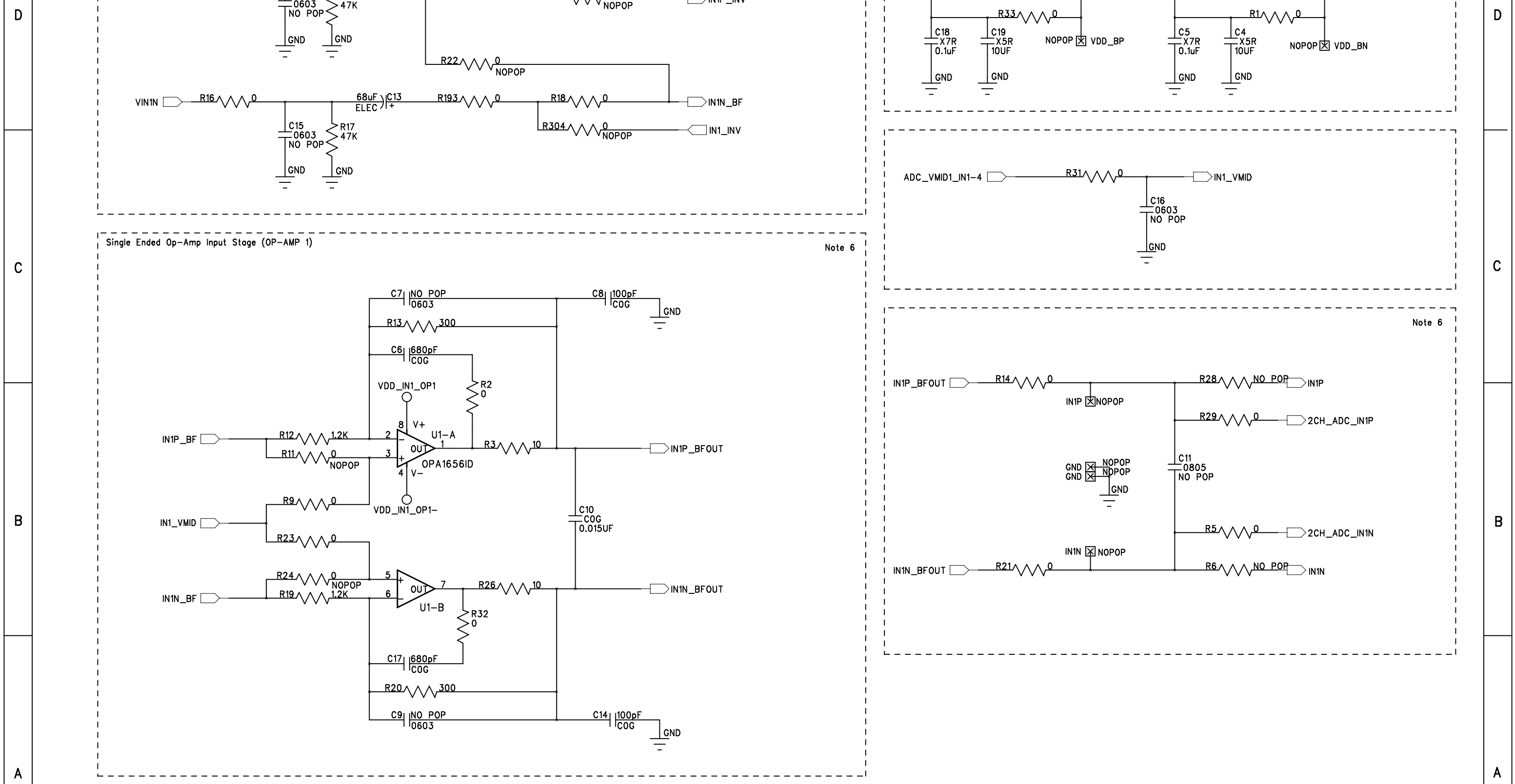
Single Ended Input Circuits

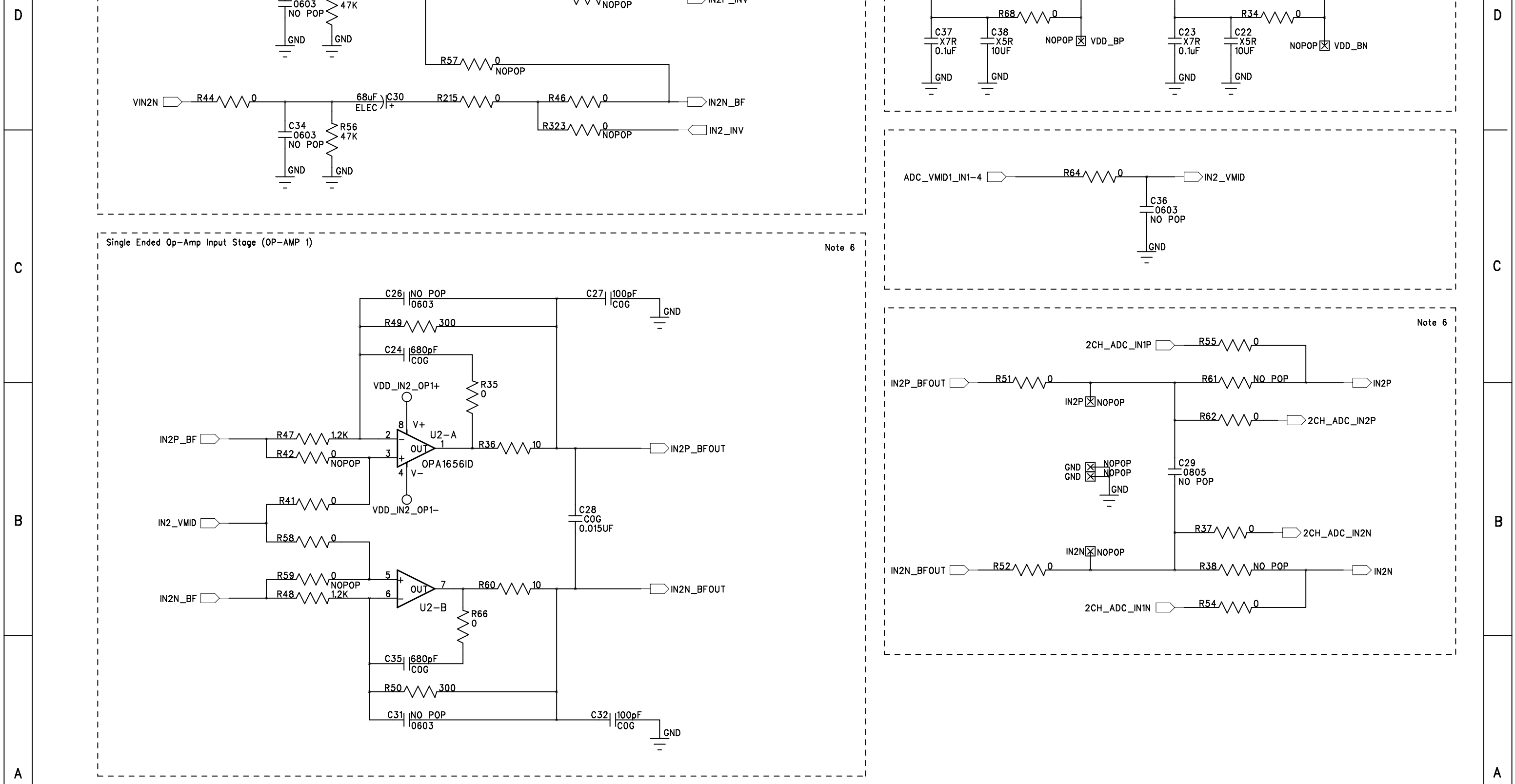
Single Ended to Differential

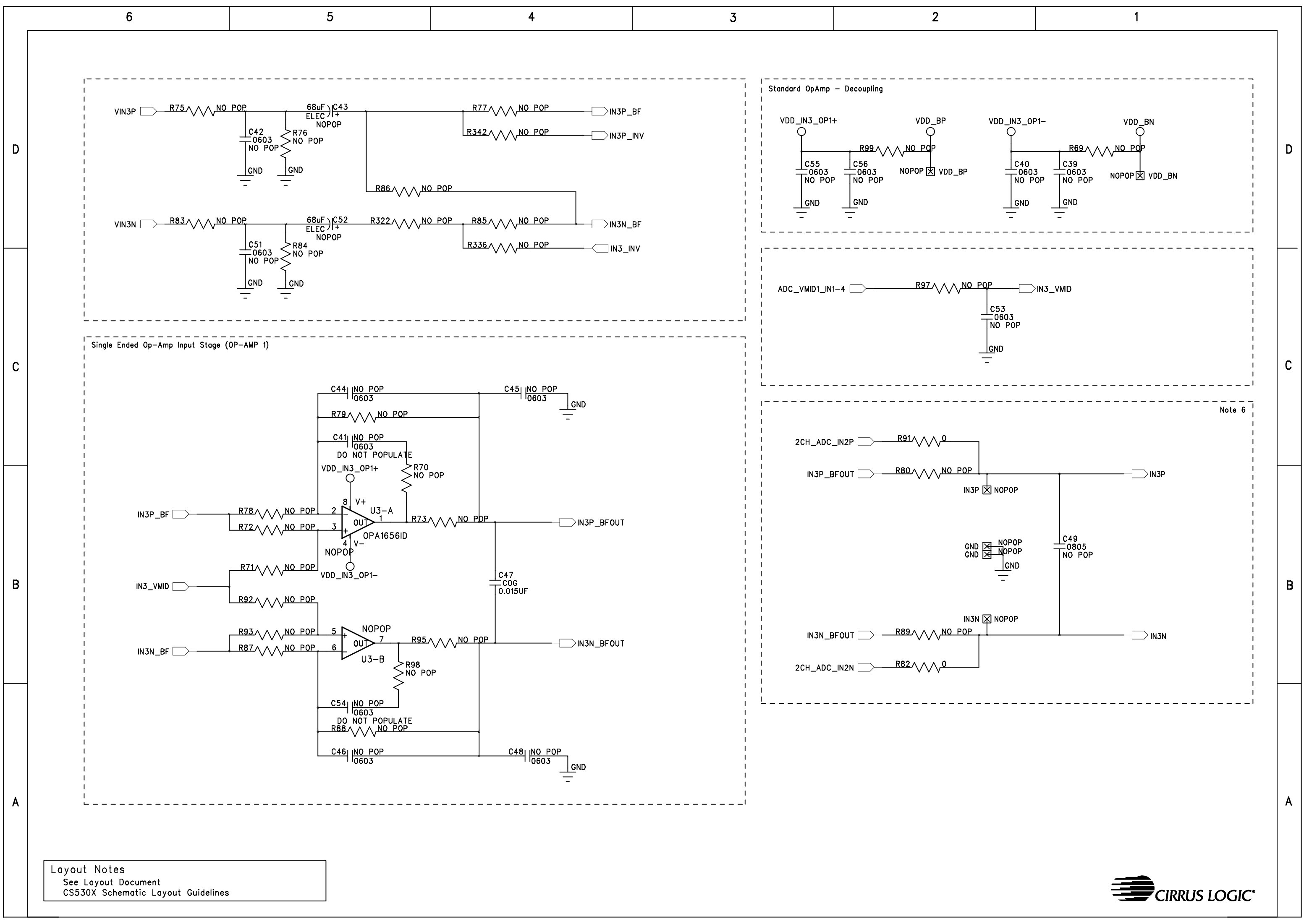


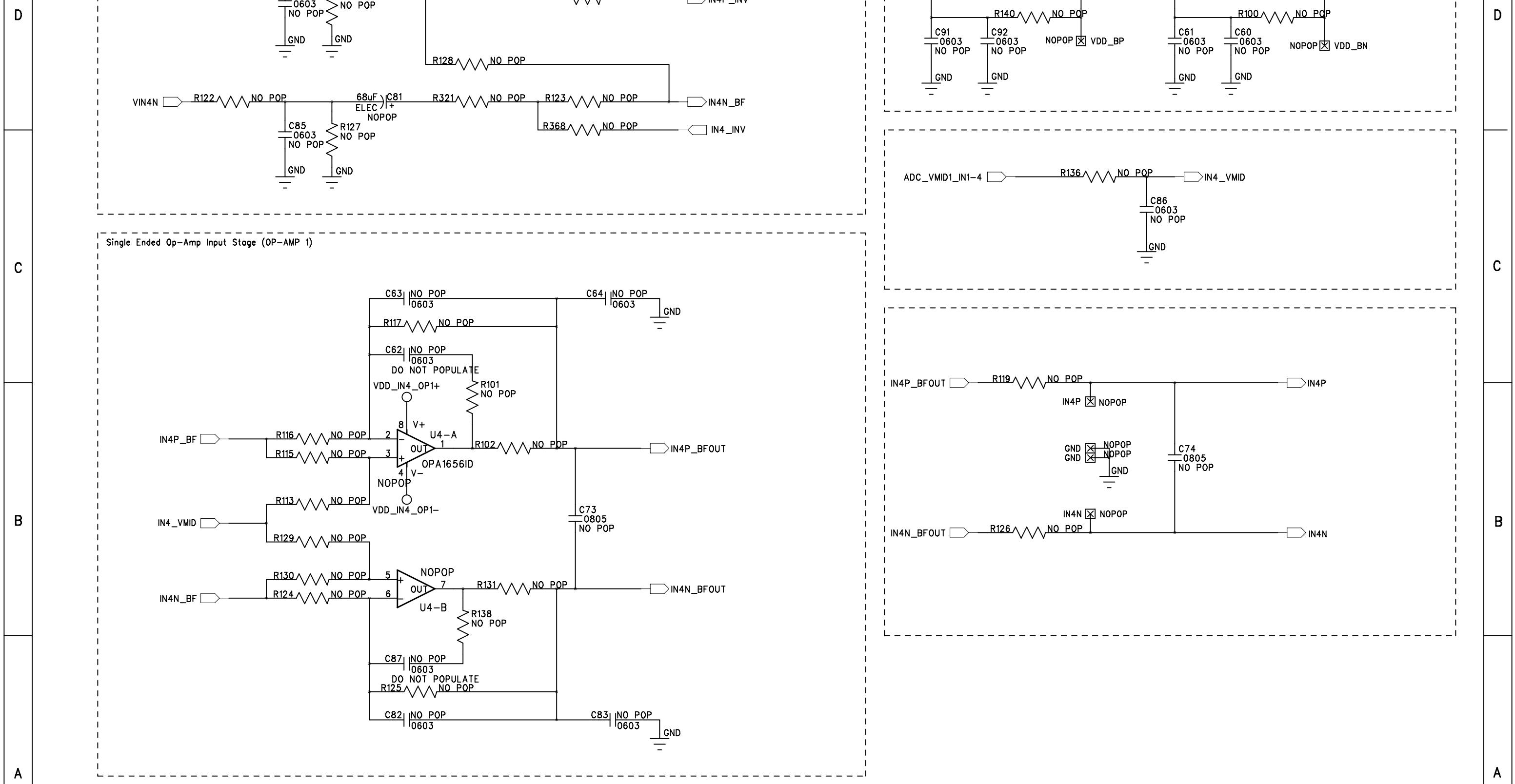
Single Ended to Differential (ADC VMID must be buffered in this use case)





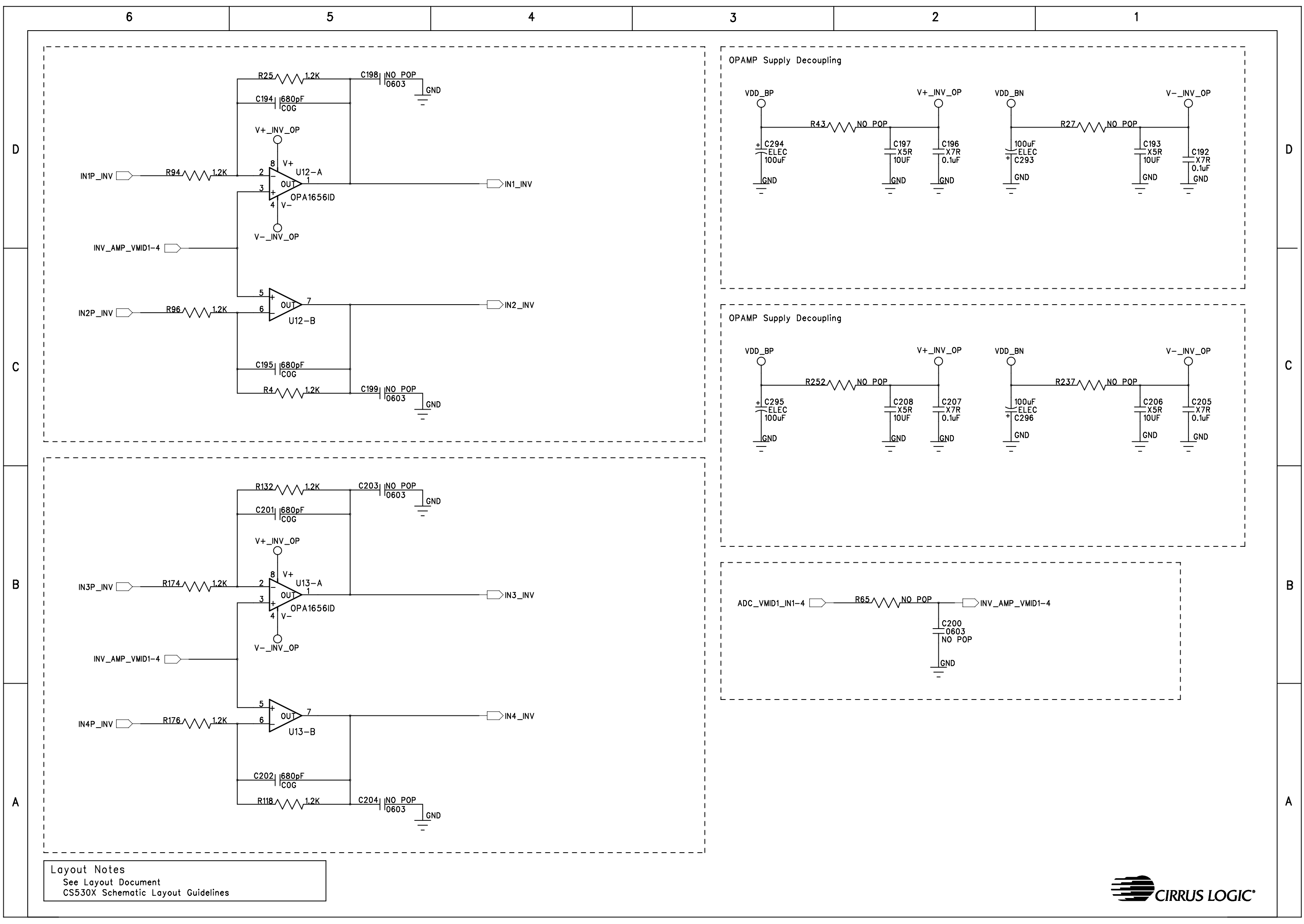




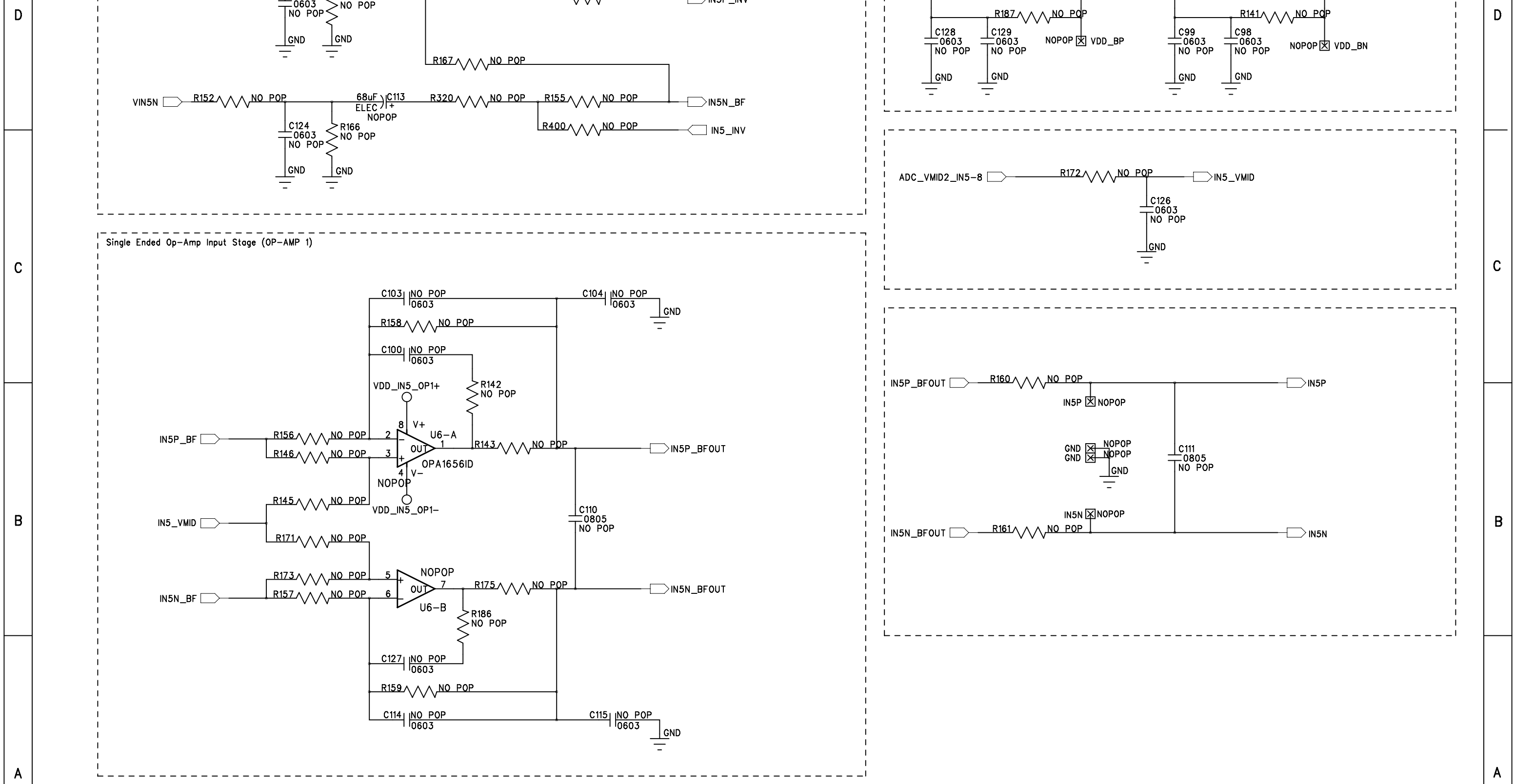


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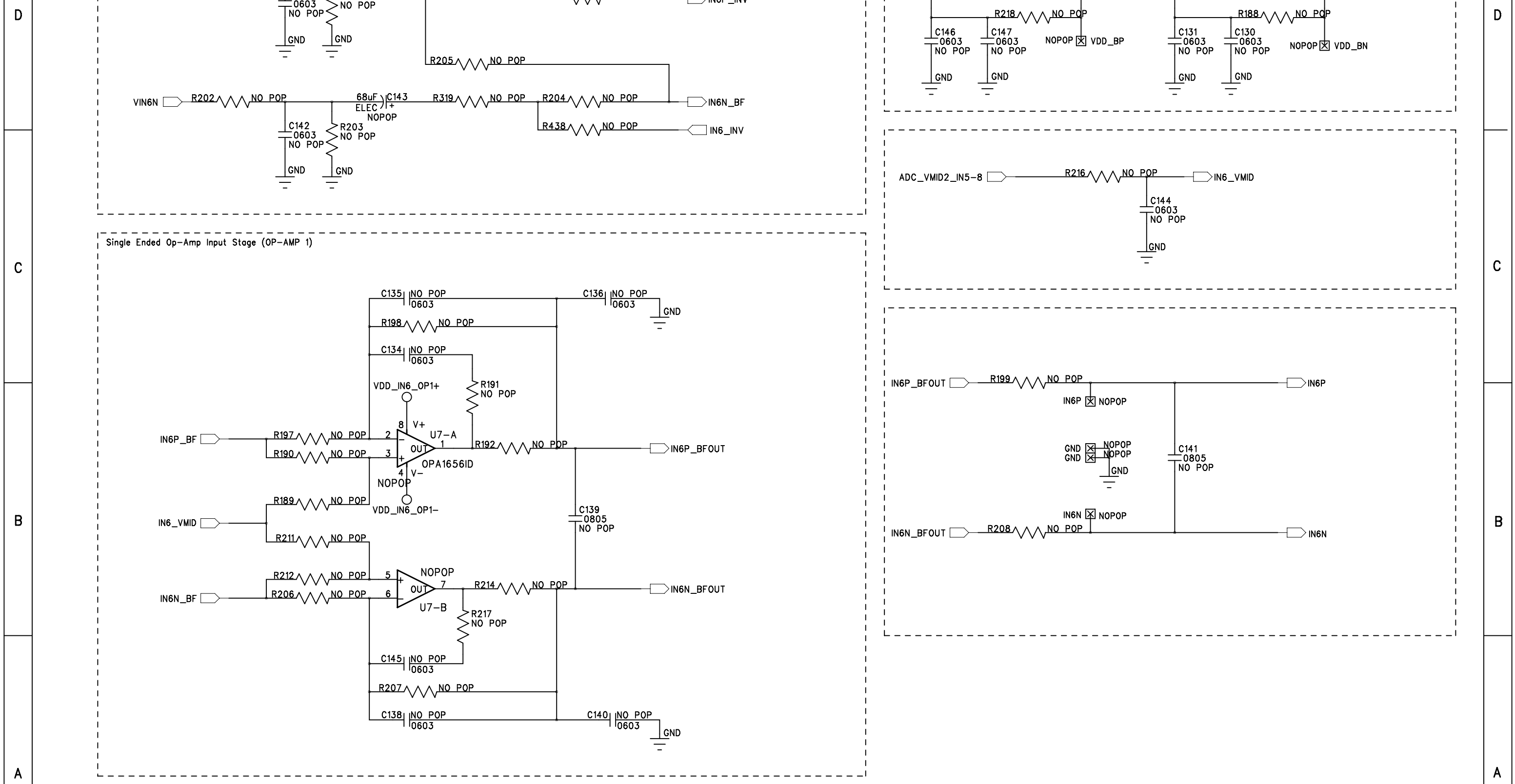


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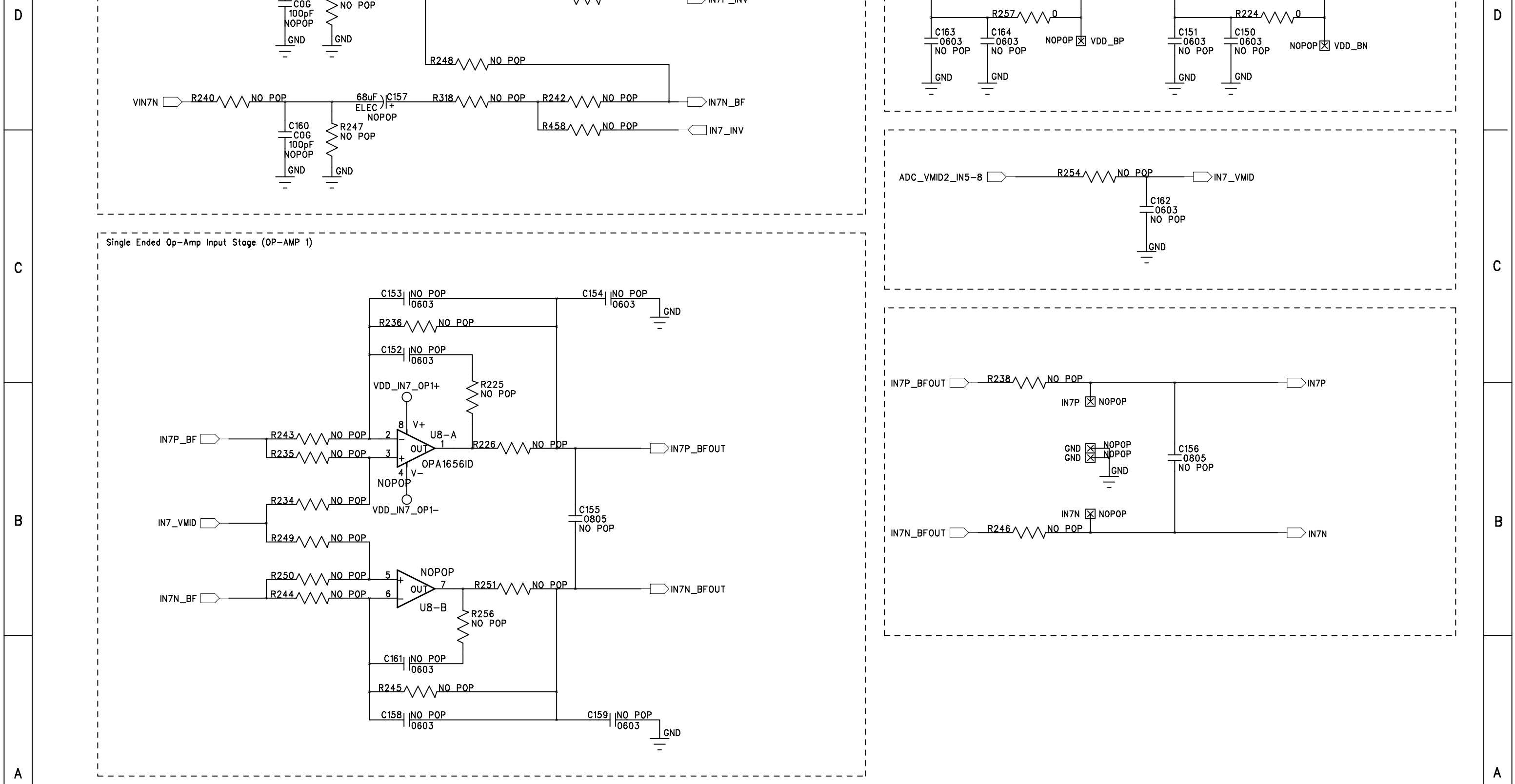


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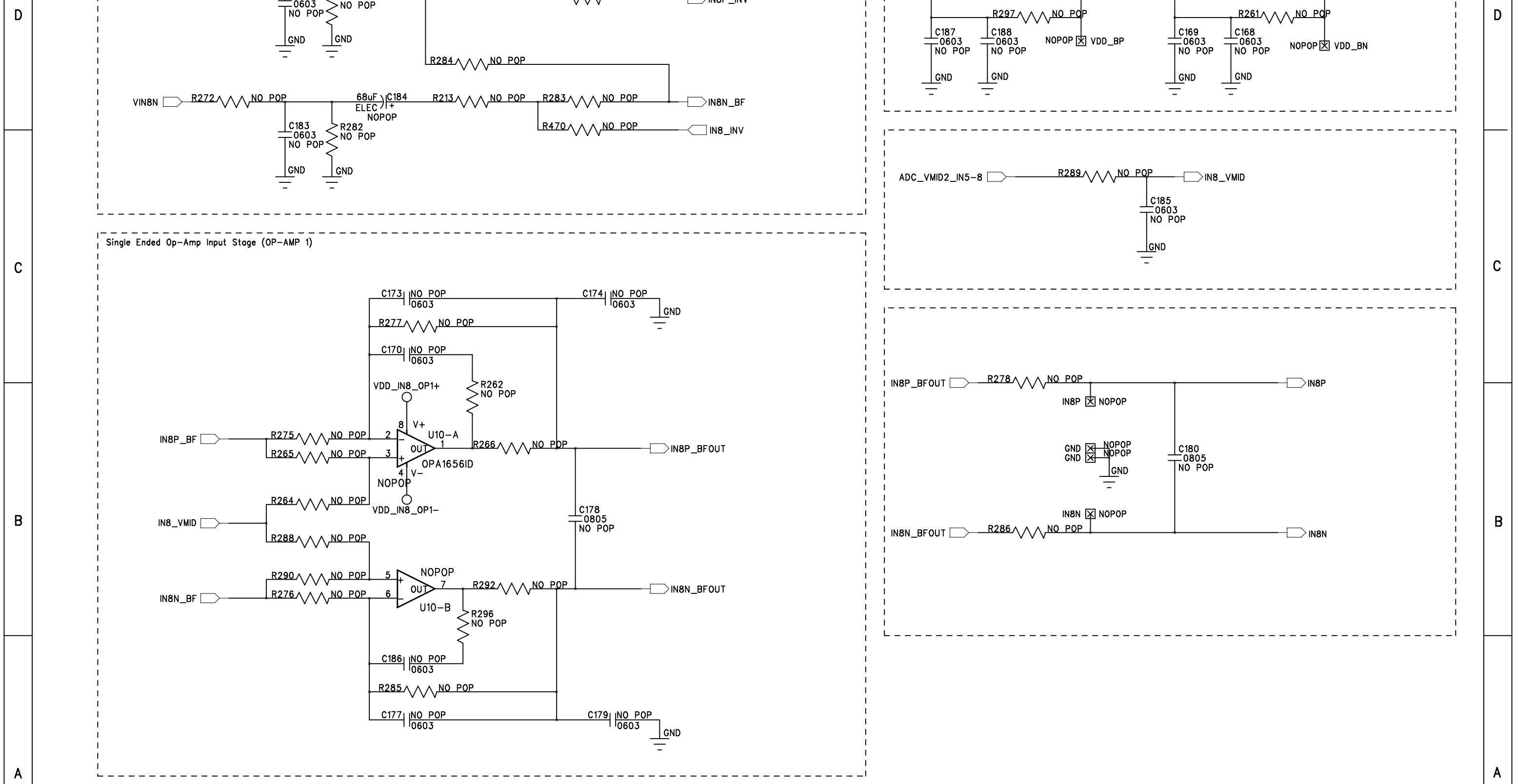


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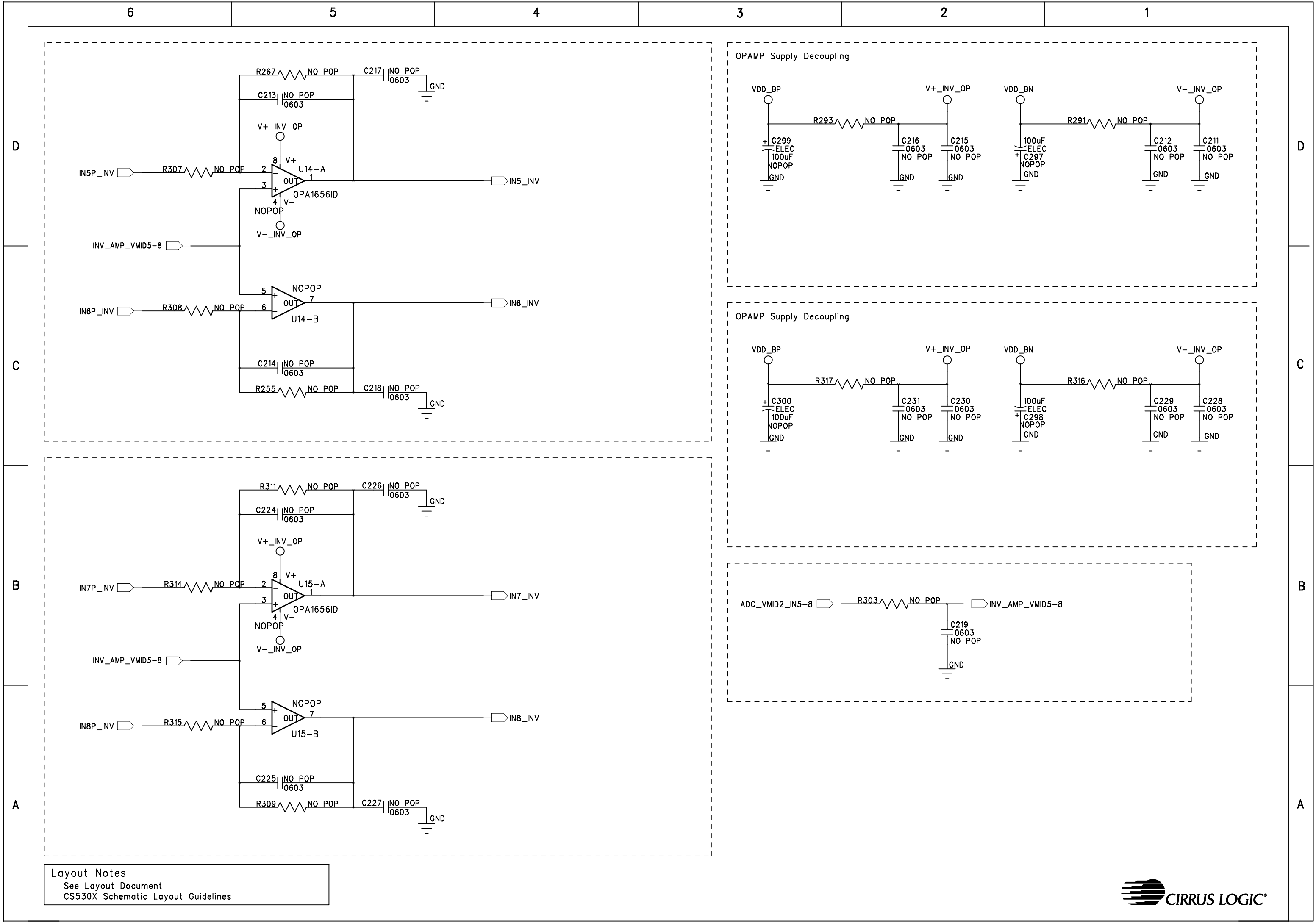
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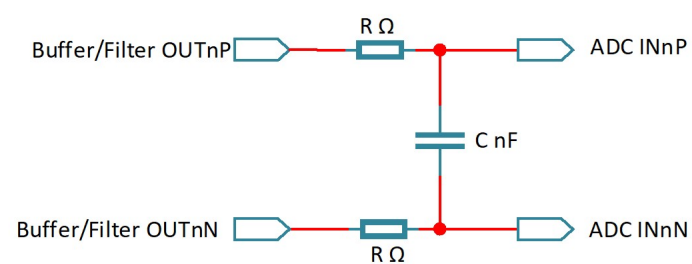




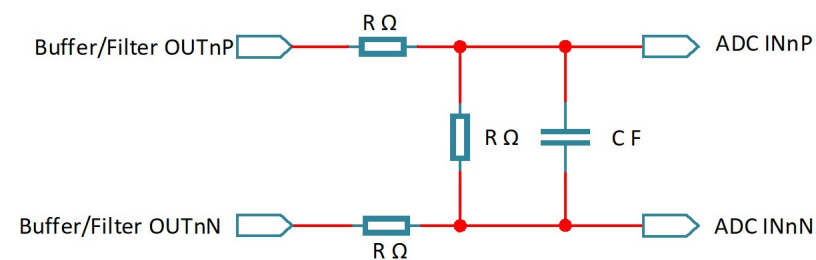
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Additional Filters After Buffer Filter

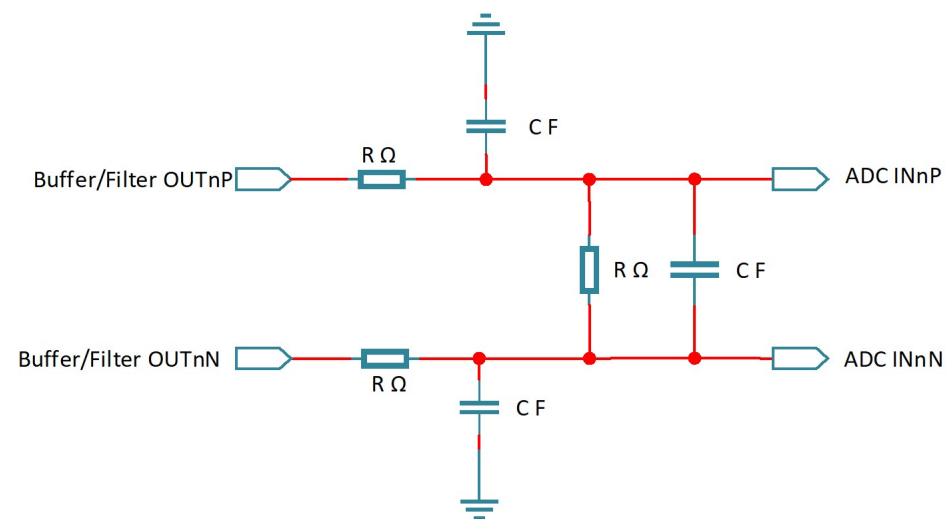
Input Filter After Buffer Filter



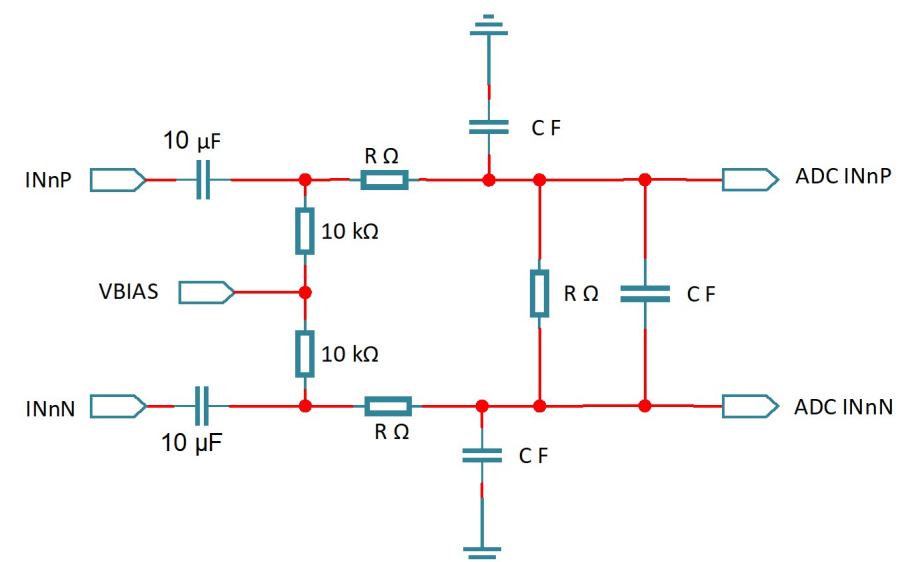
Input Filter After Buffer Filter



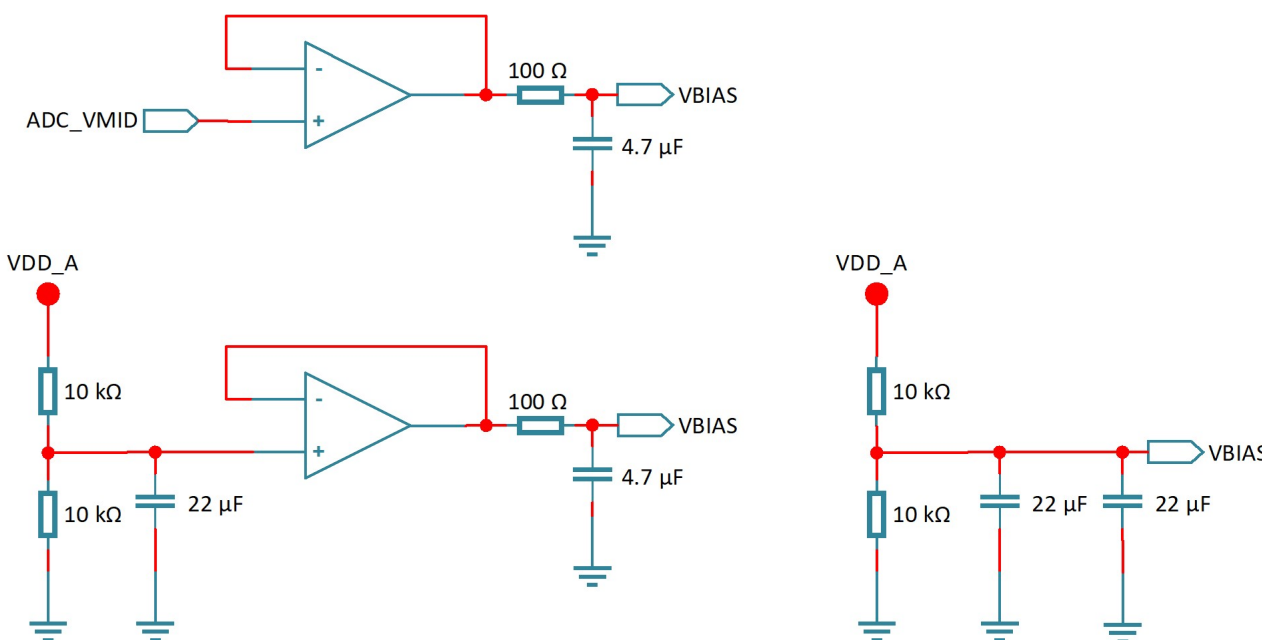
Input Filter After Buffer Filter

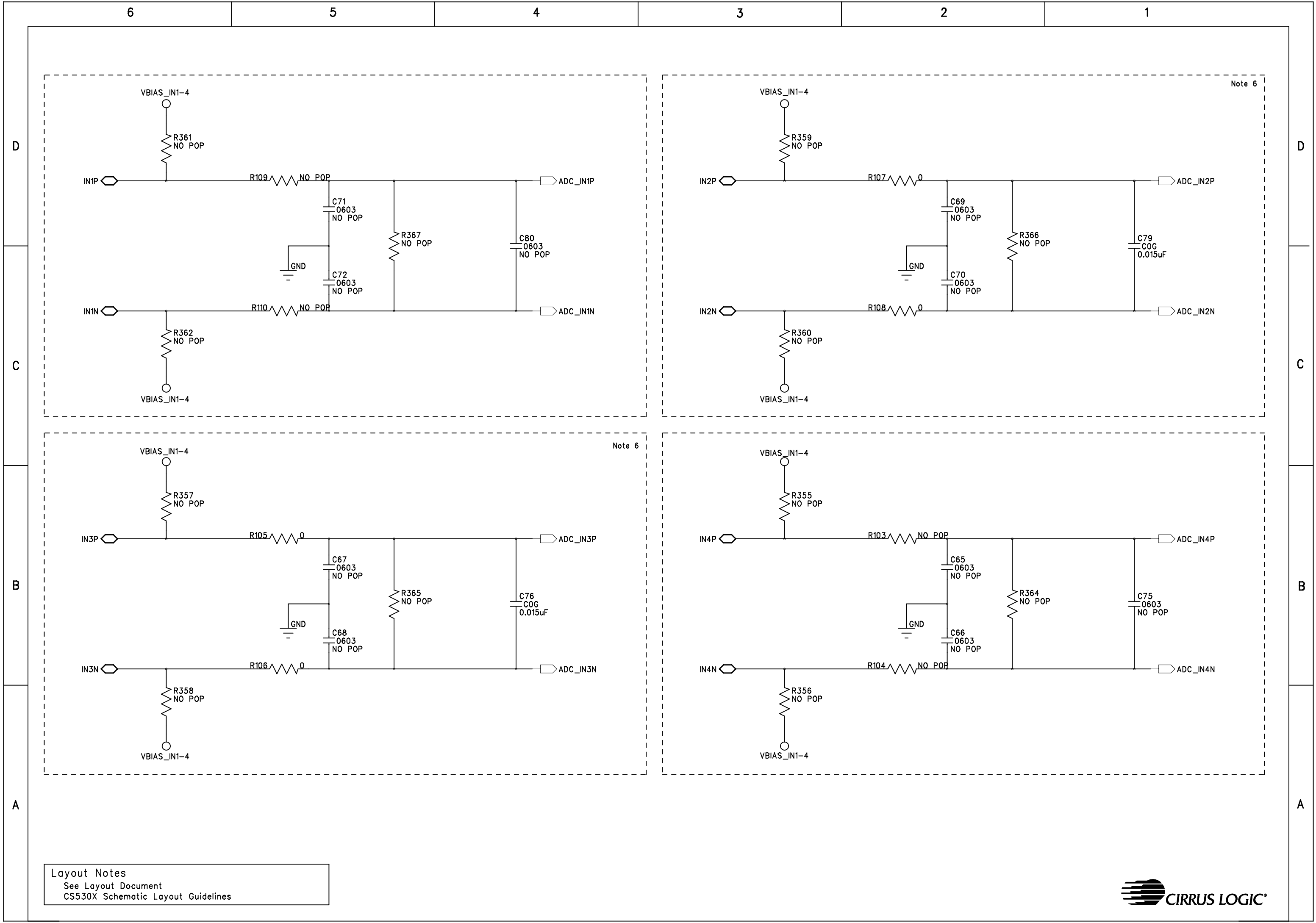


Passive Filter Input (No Buffer/Filter)



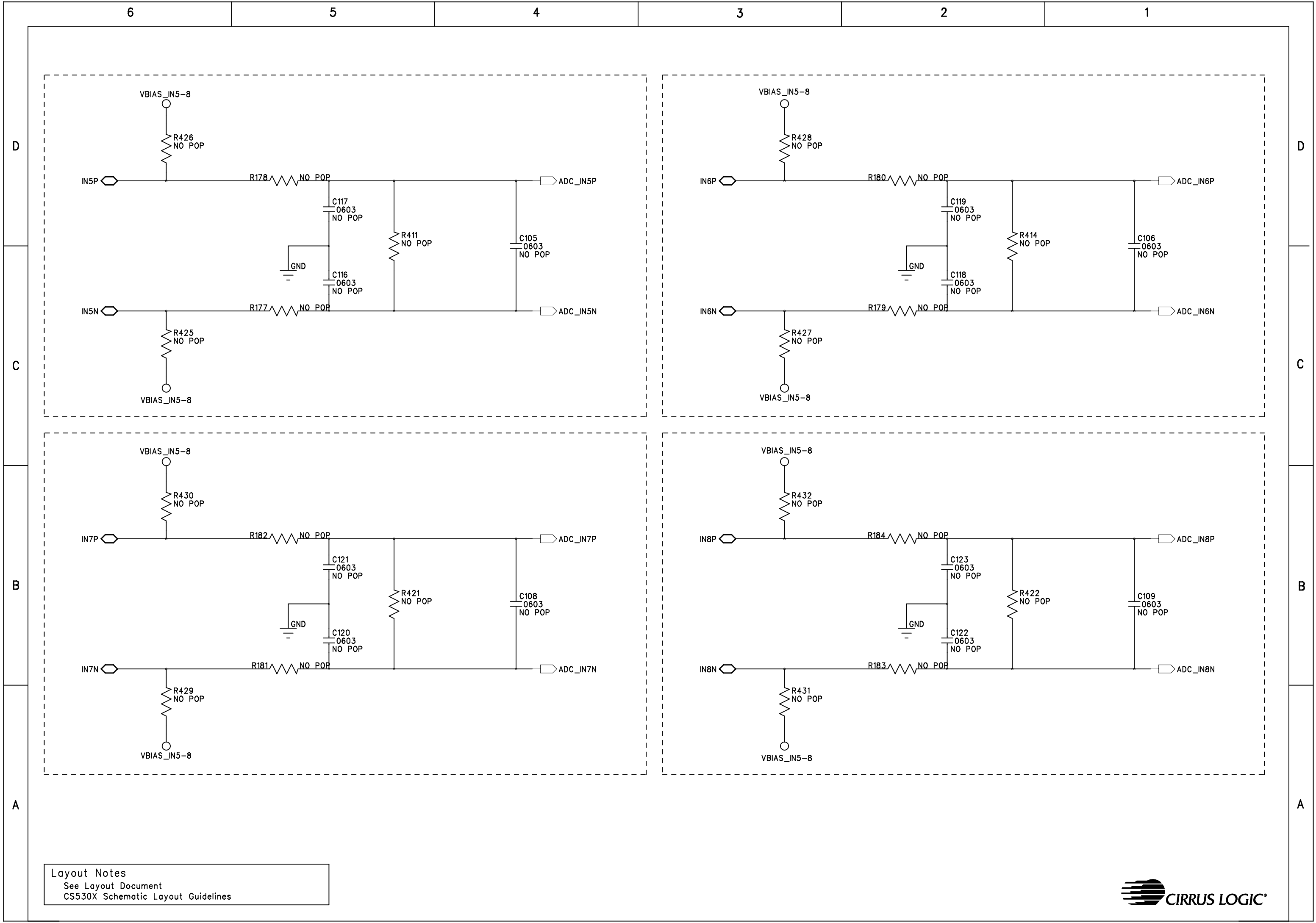
VBIAS Generation options





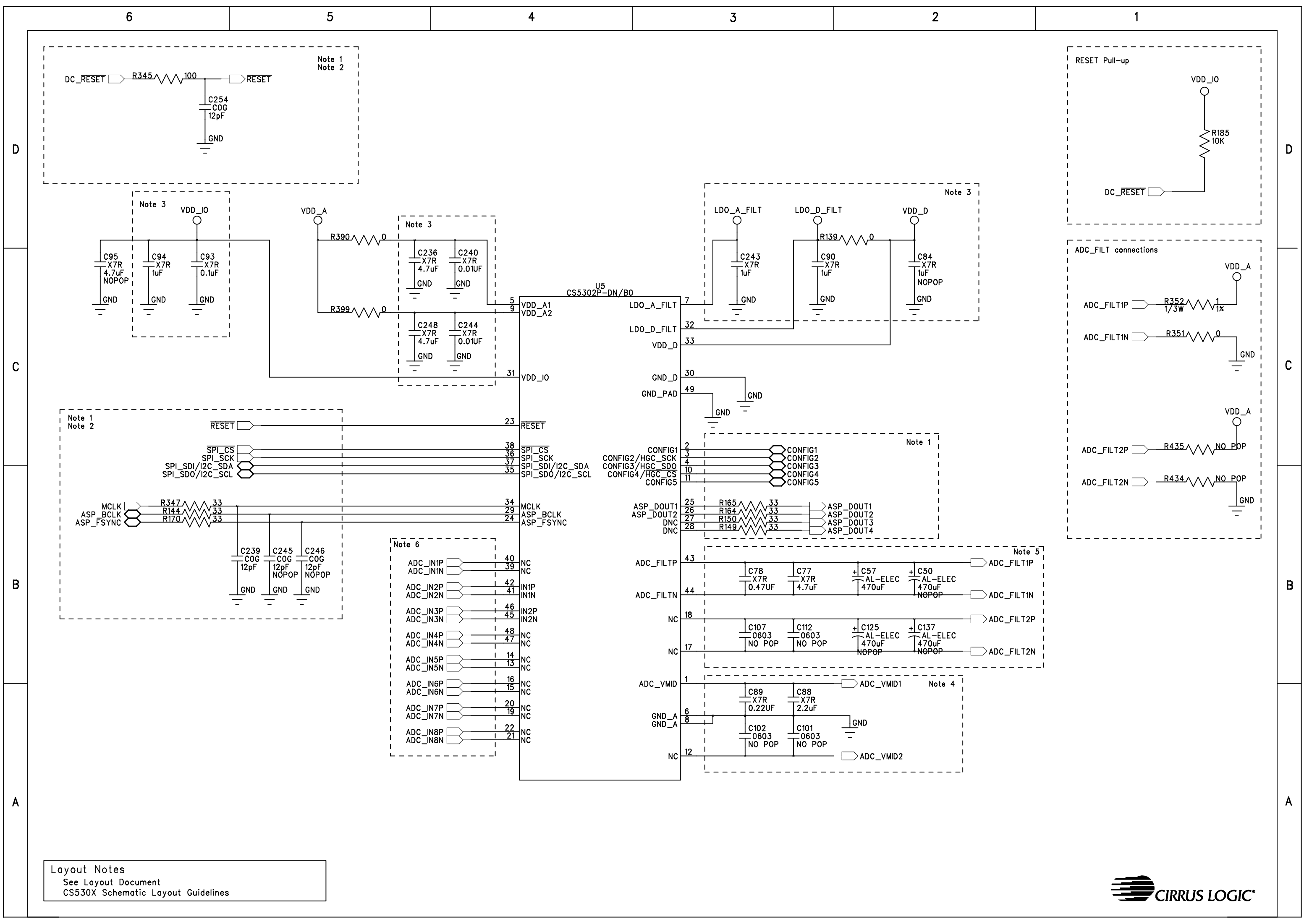
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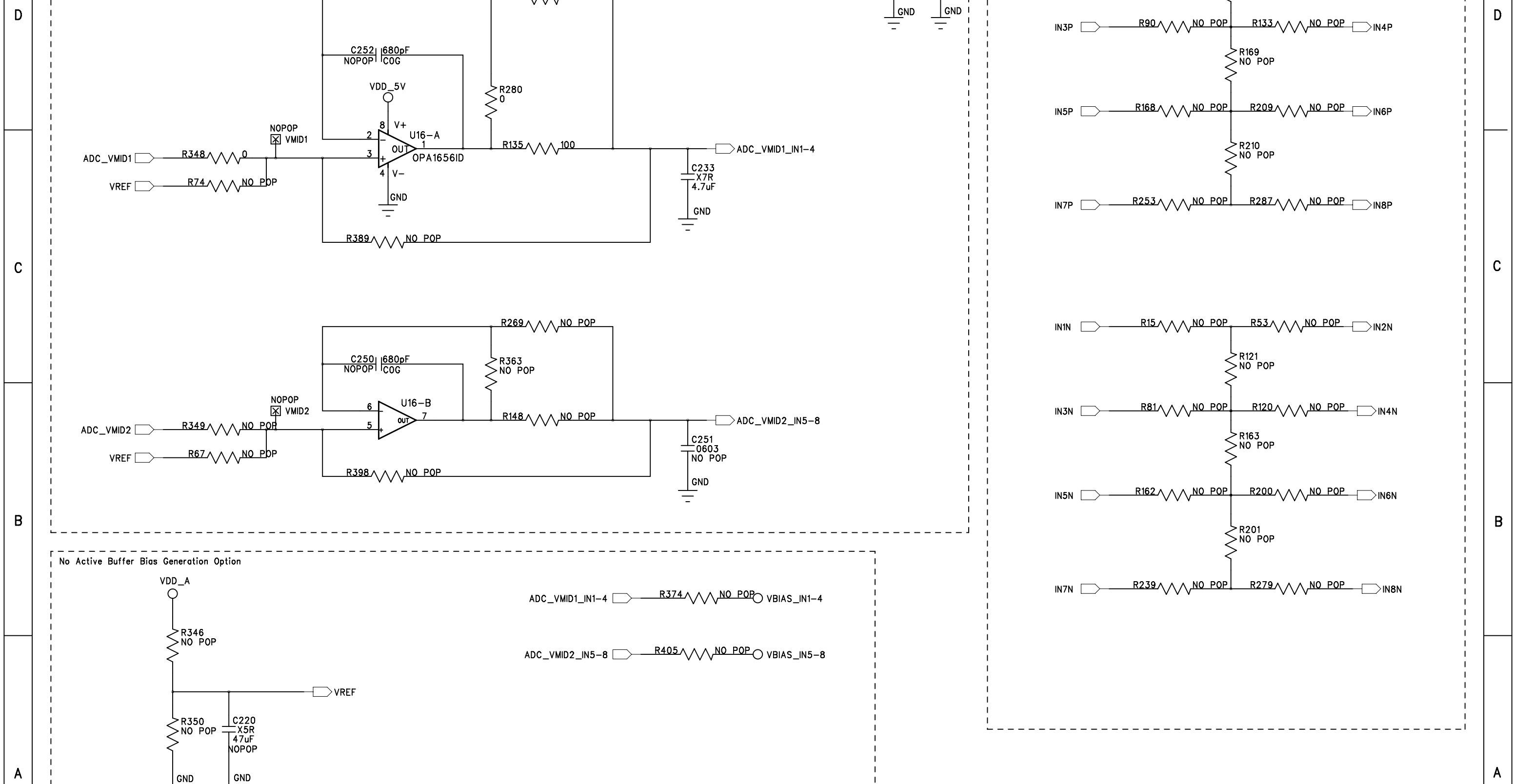
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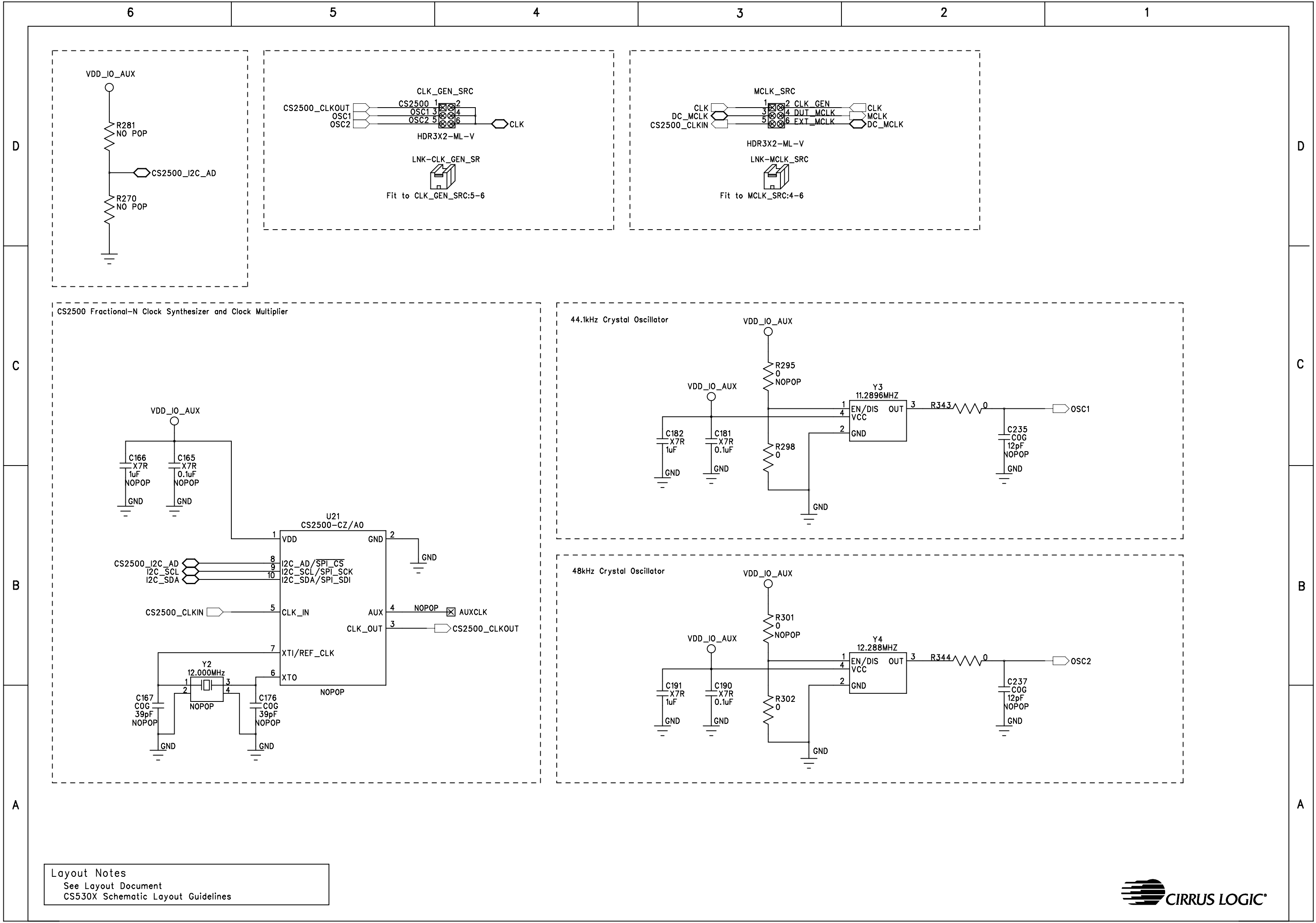




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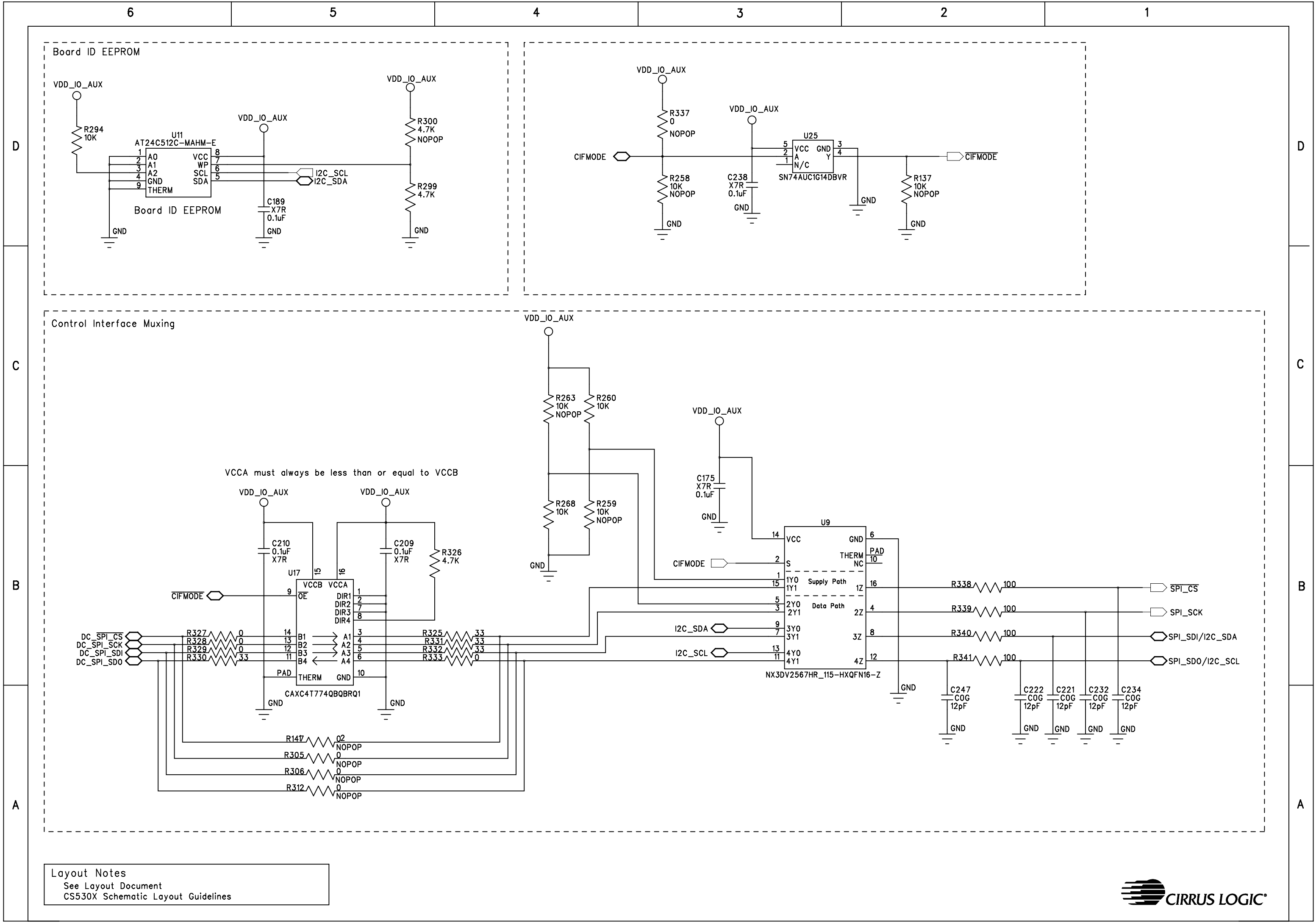
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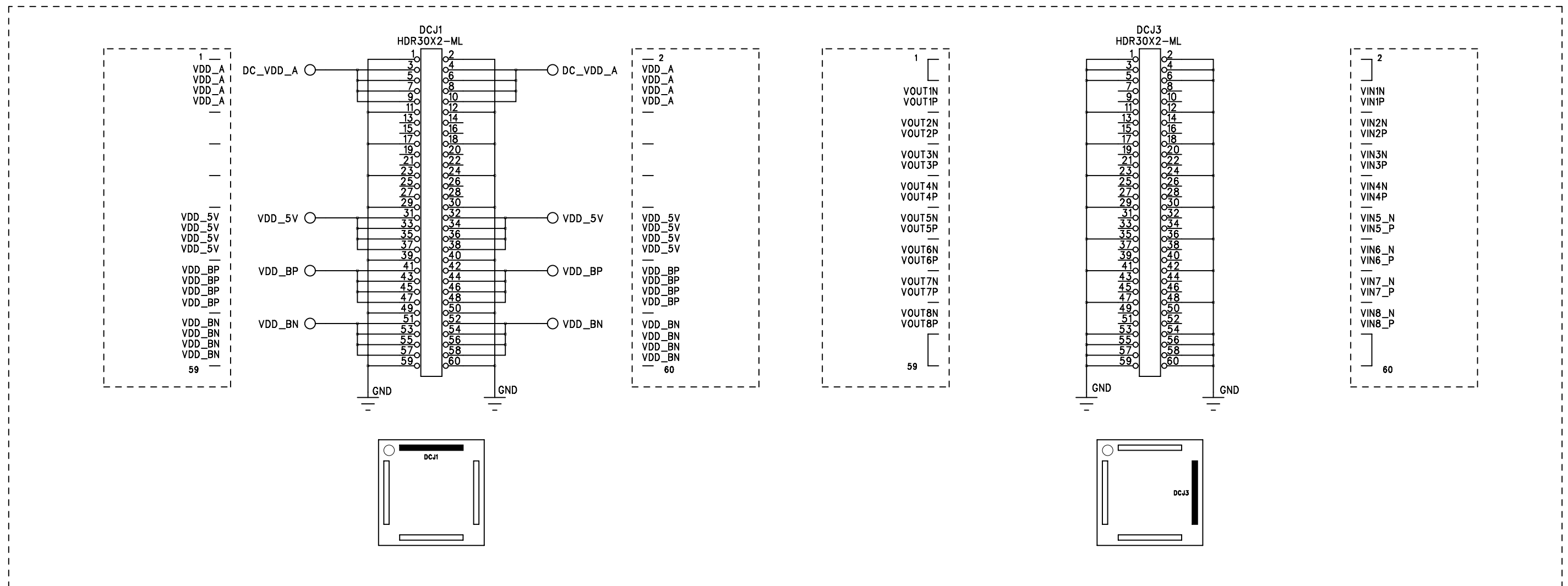
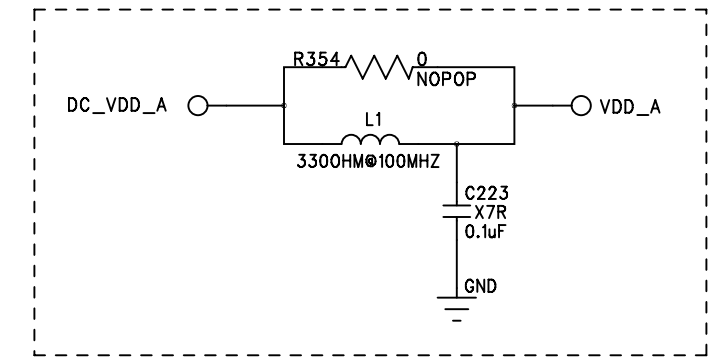
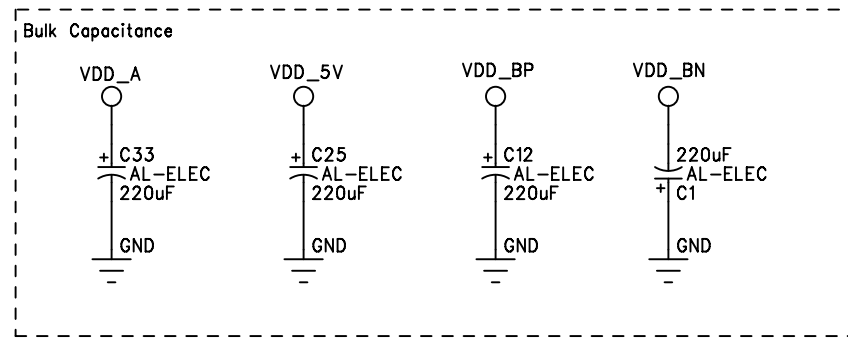
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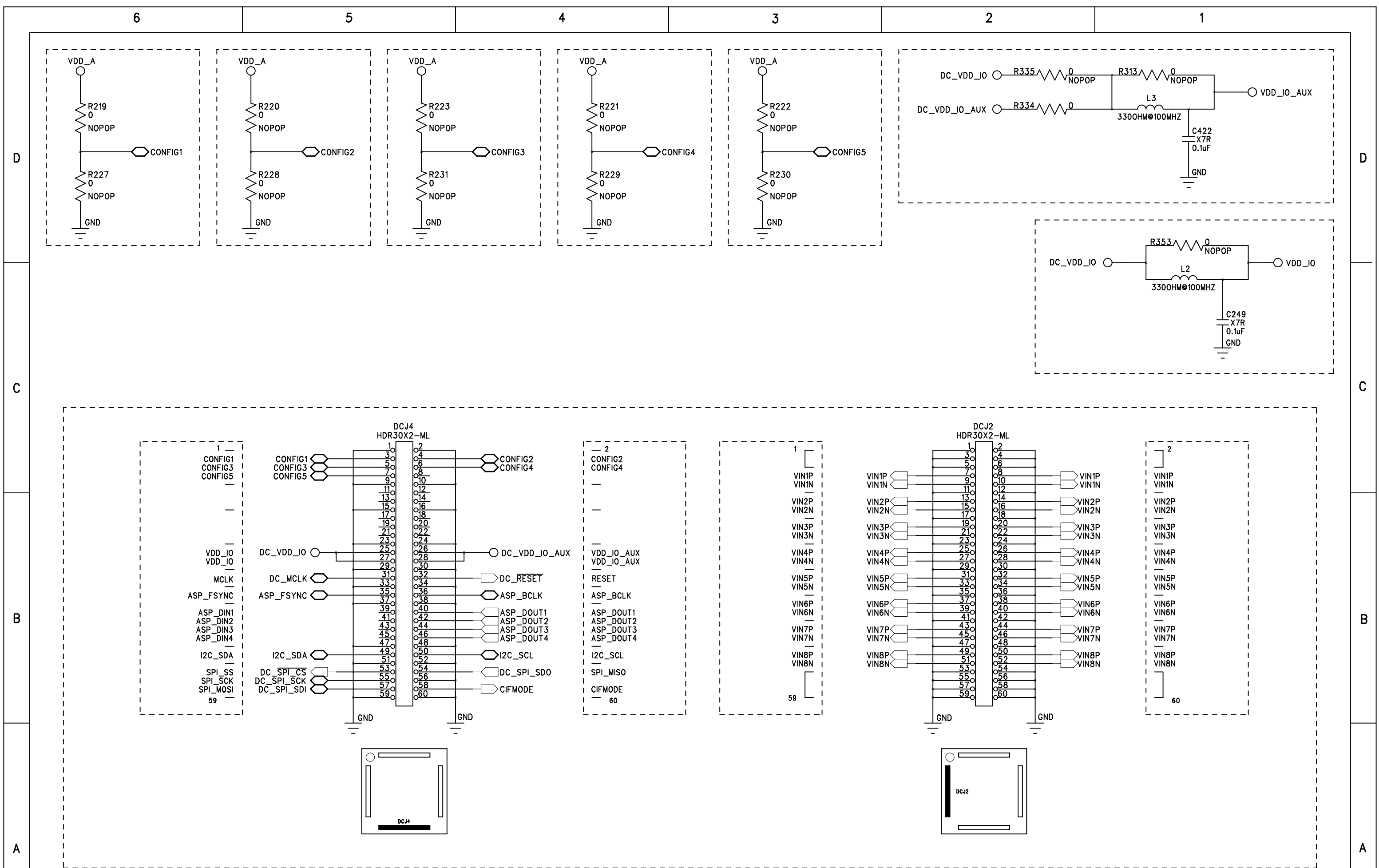


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