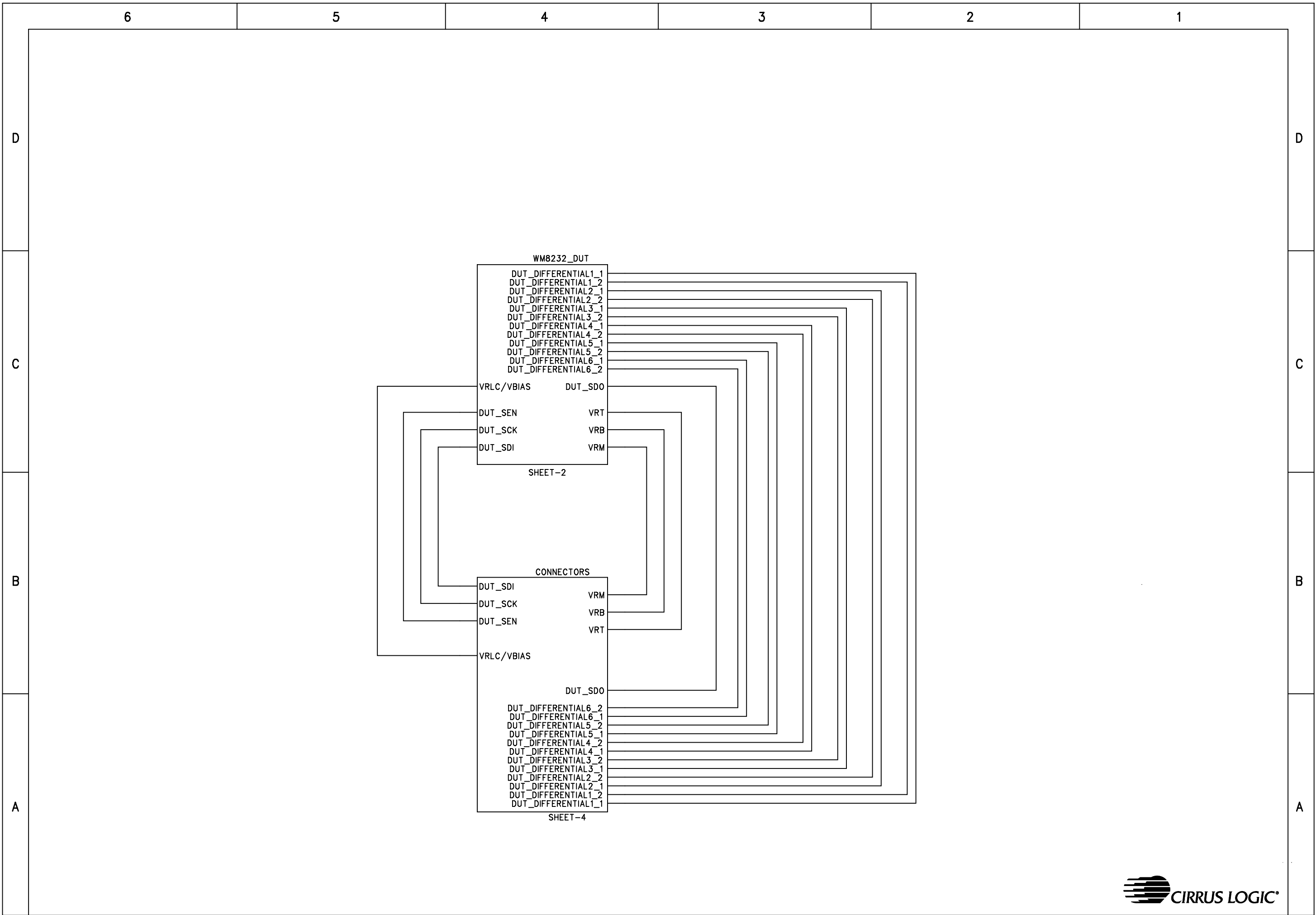




D

C

B

A

D

C

B

A

6

5

4

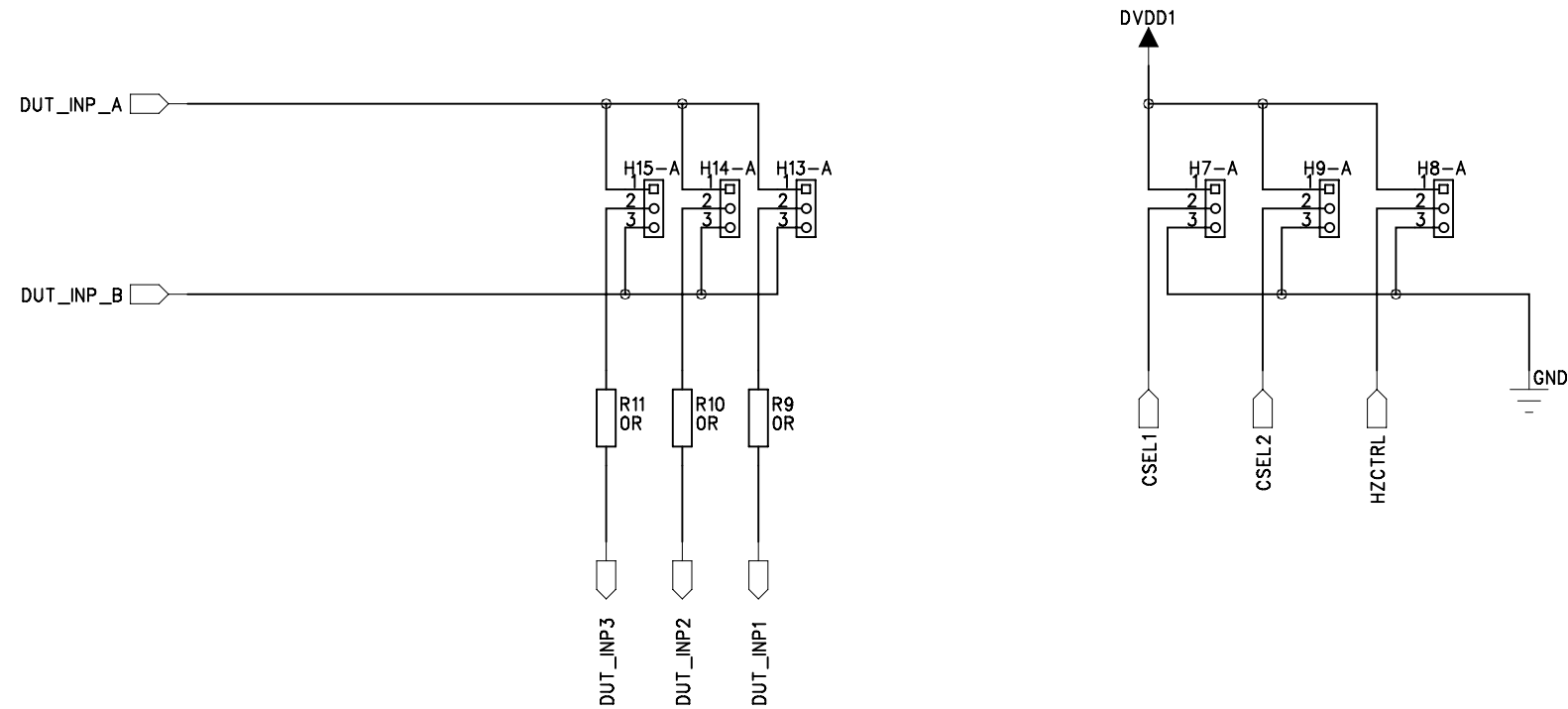
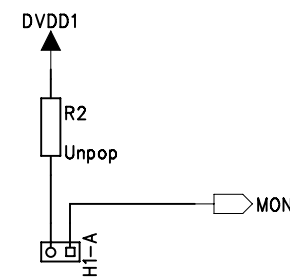
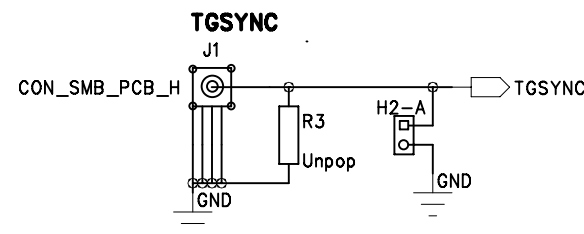
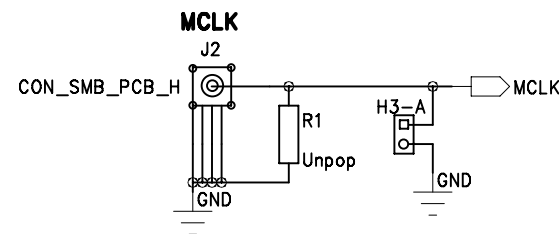
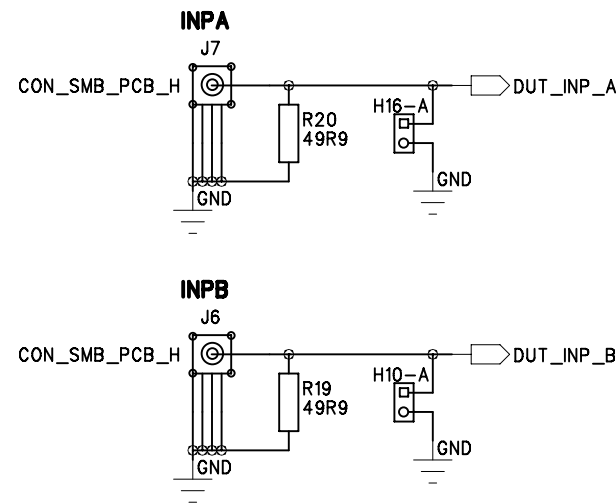
3

2

1

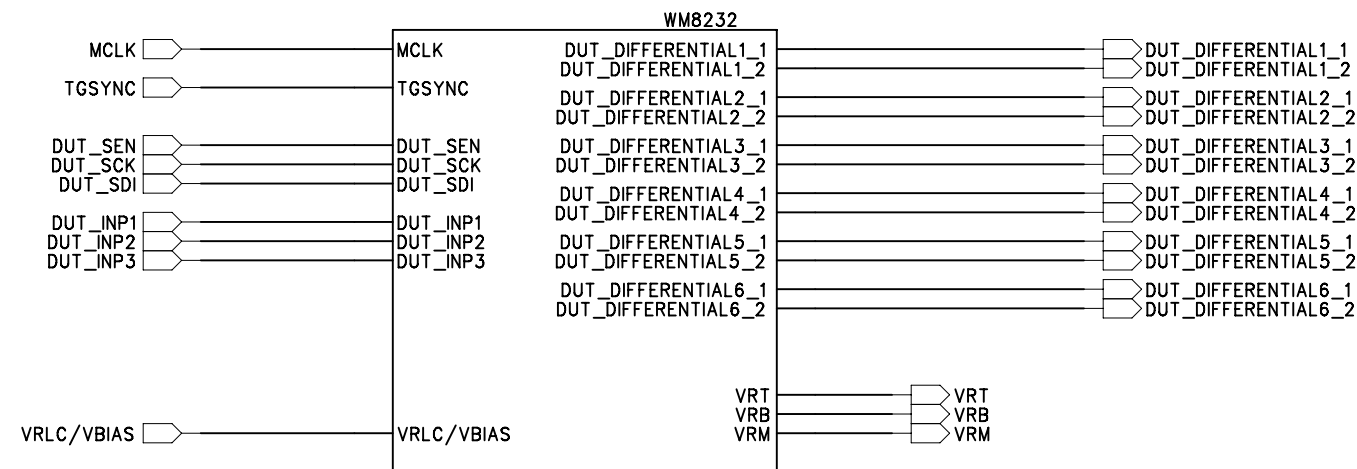
LAYOUT NOTE:

MCLK and DUT_INP should be as short as possible



LAYOUT NOTE:

DUT_INP1 to DUT_INP3 and VRMC/VBIAS should have GND guard rails.

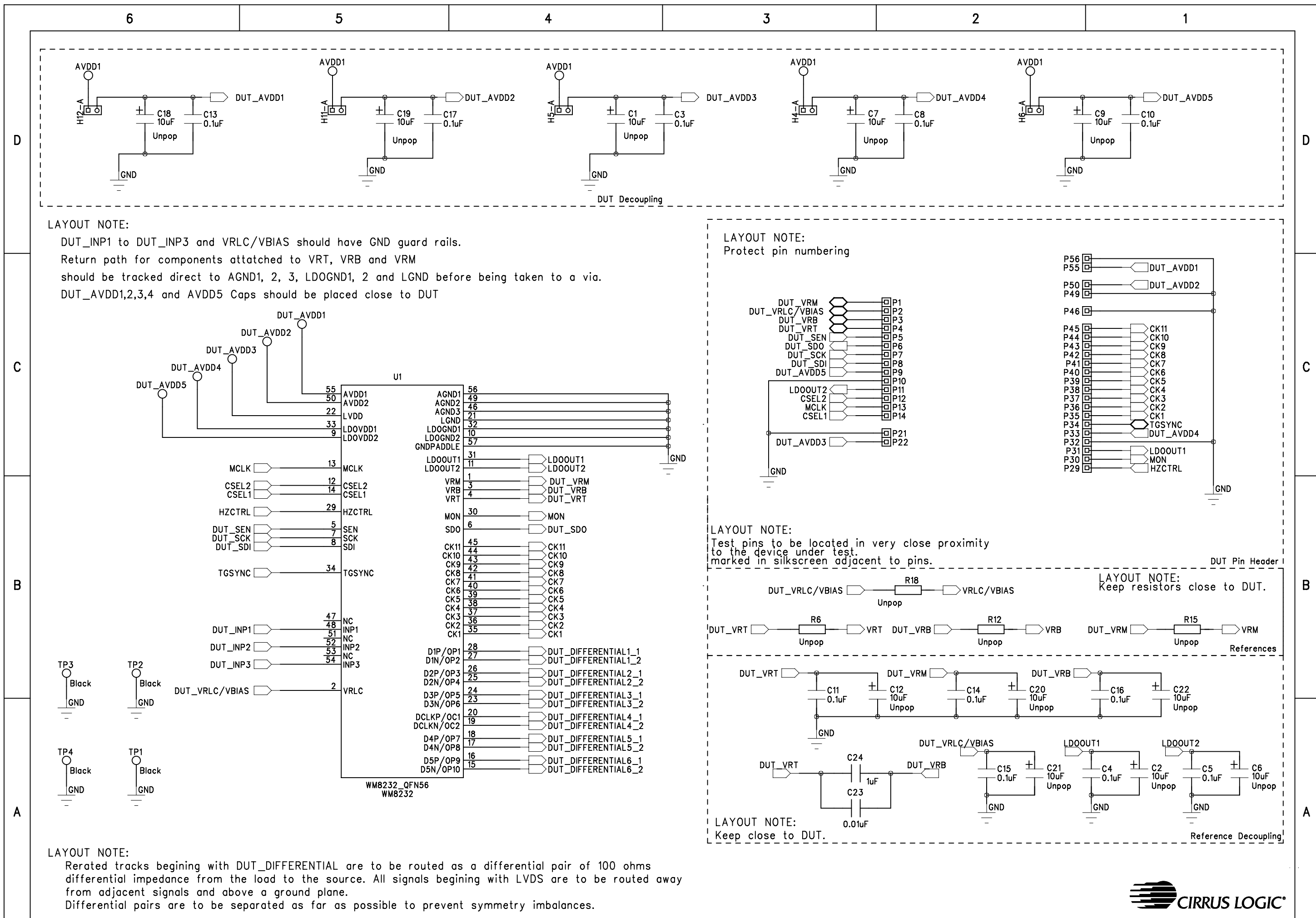


SHEET-3

LAYOUT NOTE:

Path lengths shall be short as possible.
Signal paths shall be 50 Ohm controlled impedance

Related tracks beginning with DUT_DIFFERENTIAL are to be routed as a differential pair of 100 ohms differential impedance from the load to the source. All signals beginning with LVDS are to be routed away from adjacent signals and above a ground plane.
Differential pairs are to be separated as far as possible to prevent symmetry imbalances.



6

5

4

3

2

1

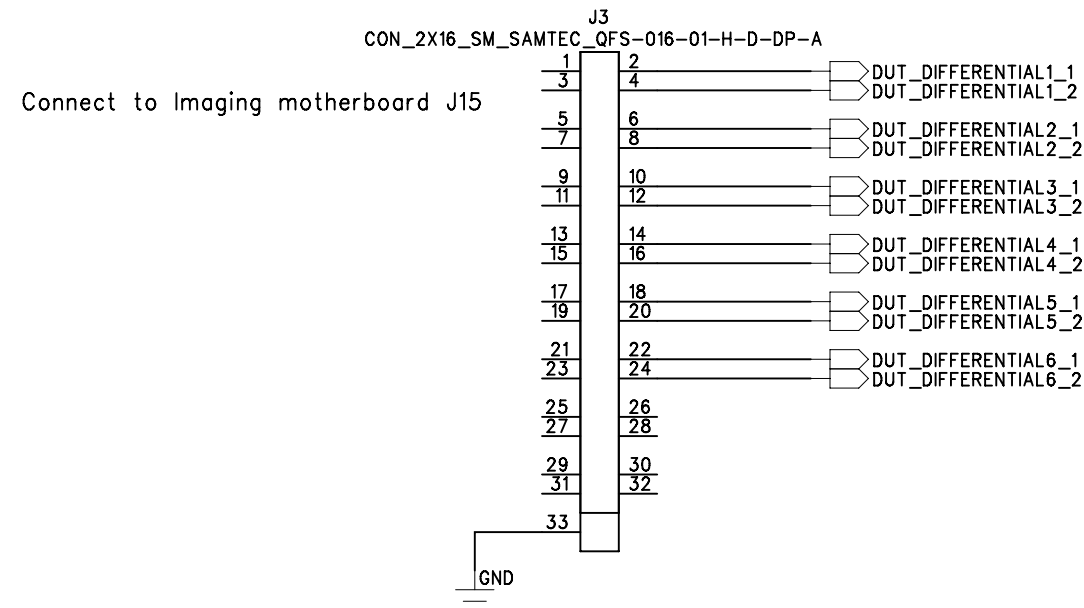
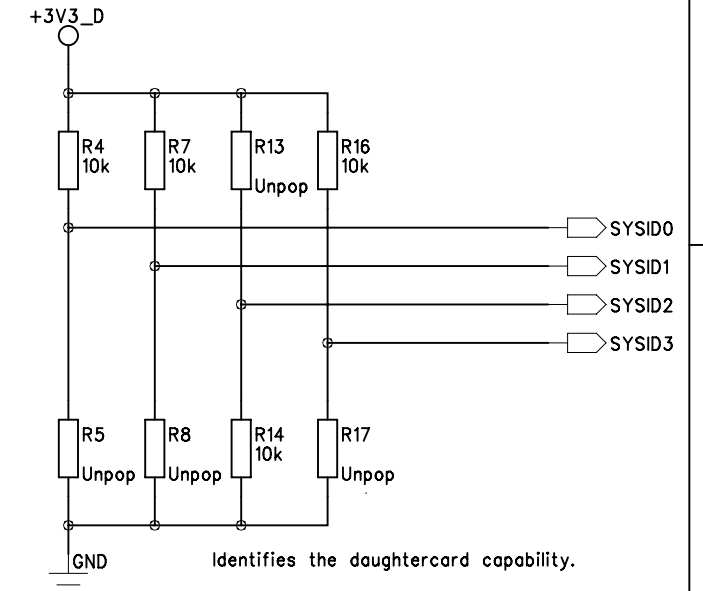
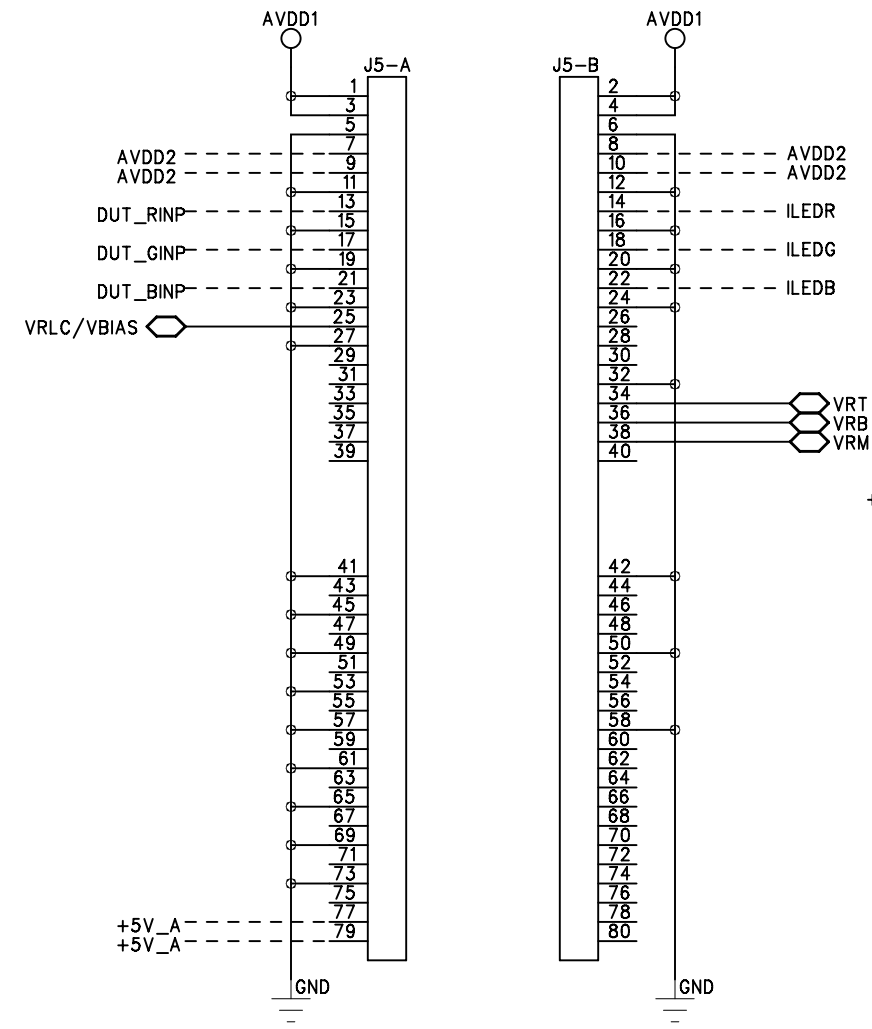
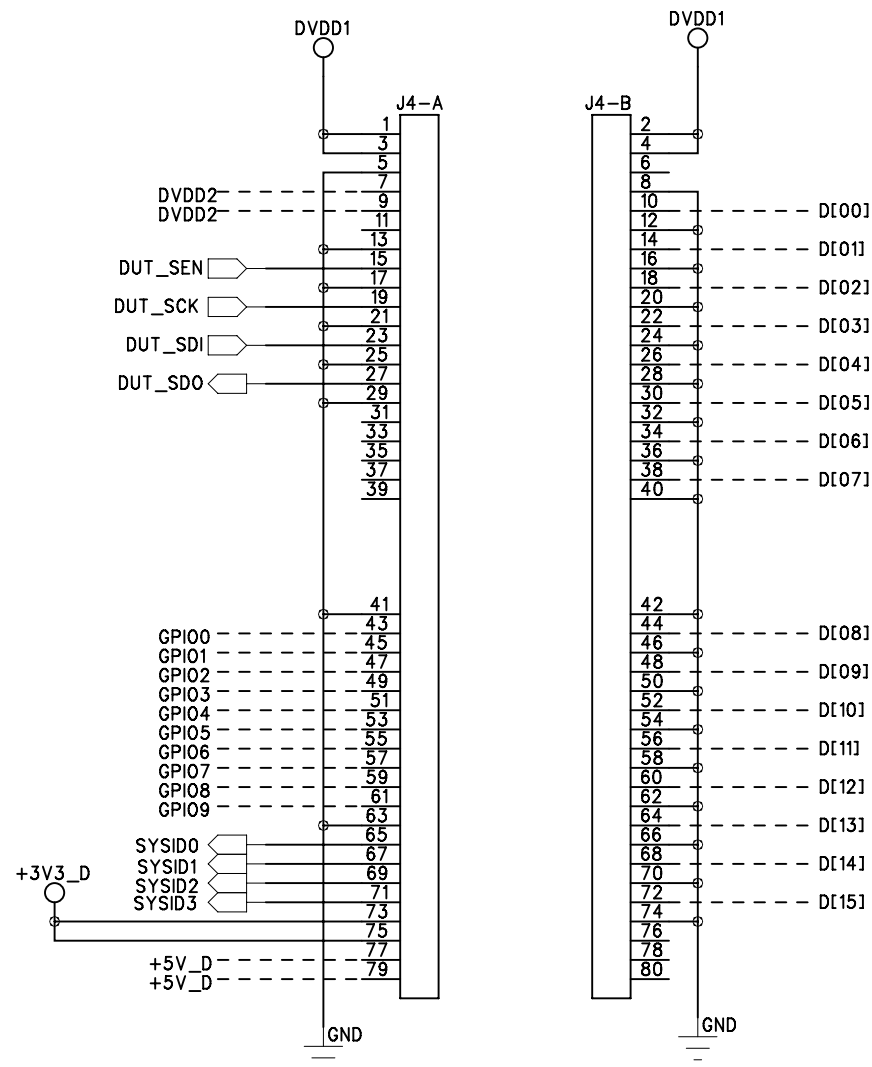
LAYOUT NOTES:

80 Way connectors and Samtec connector to be fitted to underside of PCB to match p6179 motherboard spacing.

Protect connector references.

Dotted lines indicate pins allocated for future expansion

Connector pitch to match p6109 motherboard PCB.



LAYOUT NOTE:

Related tracks beginning with DUT_DIFFERENTIAL are to be routed as a differential pair of 100 ohms differential impedance from the load to the source. All signals beginning with LVDS are to be routed away from adjacent signals and above a ground plane. Differential pairs are to be separated as far as possible to prevent symmetry imbalances.