
Increasing ADC Dynamic Range with Channel Summation

by
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1. Introduction

A commonly used technique to increase the system dynamic range of audio converters is to operate two converter channels in parallel with the same signal and sum the outputs. The summation of the correlated signals creates a 6 dB increase in signal level while the summation of the uncorrelated noise sources increases the noise level by only 3 dB. This summation effectively results in a 3 dB increase in dynamic range compared to each individual channel. This technique is most commonly associated with digital-to-analog converters but is also applicable to analog-to-digital converters; as presented at the 87th AES Convention, "An 18-bit Dual Channel Oversampling Delta-Sigma A/D Converter, with 19-bit Mono Application Example" by Clifton Sanchez of Crystal Semiconductor. In the case of an A/D converter, it may be necessary to divide each of the digital signals by two prior to summation to avoid signal overload in the processor. This approach is shown in the equations below, where A represents the signal in channel A, B the signal in channel B and e_o is the summed signal.

$$e_o = A/2 + B/2$$

$$\text{If } A = B$$

$$e_o = A/2 + A/2$$

$$e_o = A$$

Another approach, which achieves the identical mathematical results, is to invert one of the analog inputs prior to conversion and perform a subtraction of the two independent digital outputs. The advantage of this approach is that any common in-phase signal between the individual digital output signals that may be introduced during the conversion process (e_N) is cancelled in the subtraction. This approach is shown in the equations below.

$$e_o = (A + e_N) / 2 - (B + e_N) / 2$$

$$\text{If } B = -A$$

$$e_o = ((A + e_N) / 2) - ((-A + e_N) / 2)$$

$$e_o = A$$

Though applicable to any A/D converter summing channels, using either technique, to increase dynamic range is generally implemented in applications requiring the ultimate in dynamic range. As a result, this technique is generally utilized with the highest performance A/D converters that are available. This application note will demonstrate an implementation using the CS5381, which achieves 120 dB dynamic range for each individual channel in a standard two-channel configuration, to achieve 123 dB dynamic range.

2. Implementation Requirements for the CS5381

The block diagram shown in Figure 1 shows an implementation of the CS5381 A/D. Notice that the same analog signal is applied to each of the A/D converters within the CS5381. The required mathematical operation is then performed in either a Digital Signal Processor (DSP) or Field Programmable Gate Array (FPGA).

It is very important to note that the addition (or subtraction) must be performed with synchronously sampled and time aligned data pairs. Within the serial audio interface, the Left followed by Right channel data pairs are synchronously sampled data. However, the Right followed by Left channel data pairs are shifted in time by one sample period relative to each other and the addition or subtraction of these pairs will produce erroneous results. Please refer to the Cirrus Logic application note AN282 “The 2-Channel Audio Interface: A Tutorial” for more information concerning the serial audio interface and synchronously sampled data pairs.

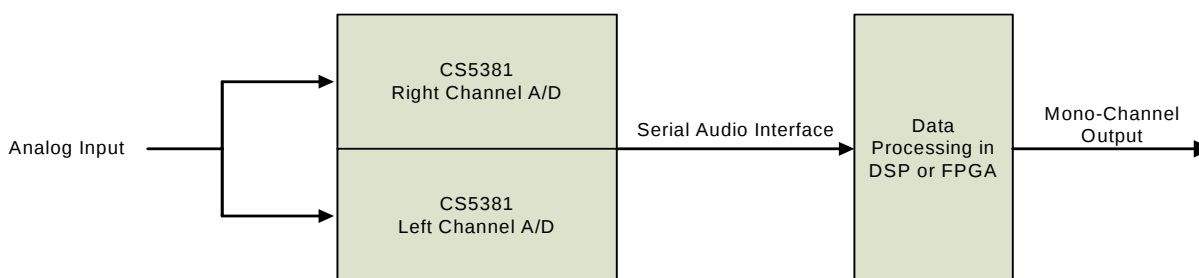


Figure 1. Mono-Mode Block Diagram

3. Recommended Analog Input Buffers for the CS5381 in Mono-Mode

An implementation with the CS5381 requires separate input buffer stages for the differential analog inputs. A single buffer driving both differential inputs has been shown to result in an unacceptable level of distortion. The recommended buffer topologies are nearly identical to that shown on the CS5381 evaluation board, CDB5381. The schematic in Figure 2 is a suggested buffer implementation for the equation $e_o = A/2 + B/2$. Notice that the AIN+ connection is routed to the AINR+ and the AINL+, and the AIN- connection is routed to the AINR- and the AINL- which results in the signals being in-phase.

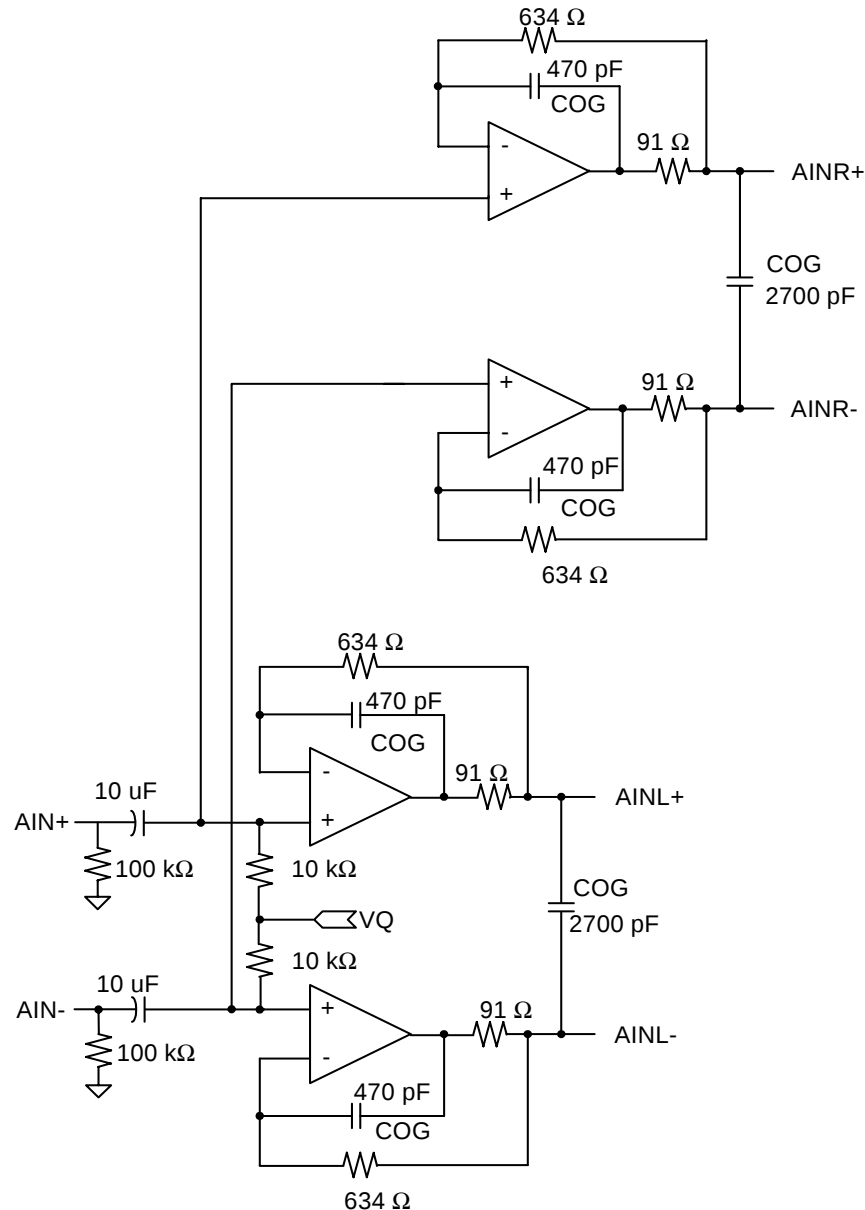


Figure 2. CS5381 Recommended Buffer Implementation for Non-inverting Configuration

3.1 The Subtraction Approach

The schematic in Figure 3 is a suggested buffer implementation for the analog inversion with digital subtraction technique, $e_o = (A / 2) - (B / 2)$. The analog inversion can be easily implemented in the connections to the differential A/D inputs where the AIN+ connection is routed to the AINR- and the AINL+, and the AIN- connection is routed to the AINR+ and the AINL-, as shown in Figure 3. This cross connection of the analog inputs results in the inversion of the Right channel input relative to the Left channel.

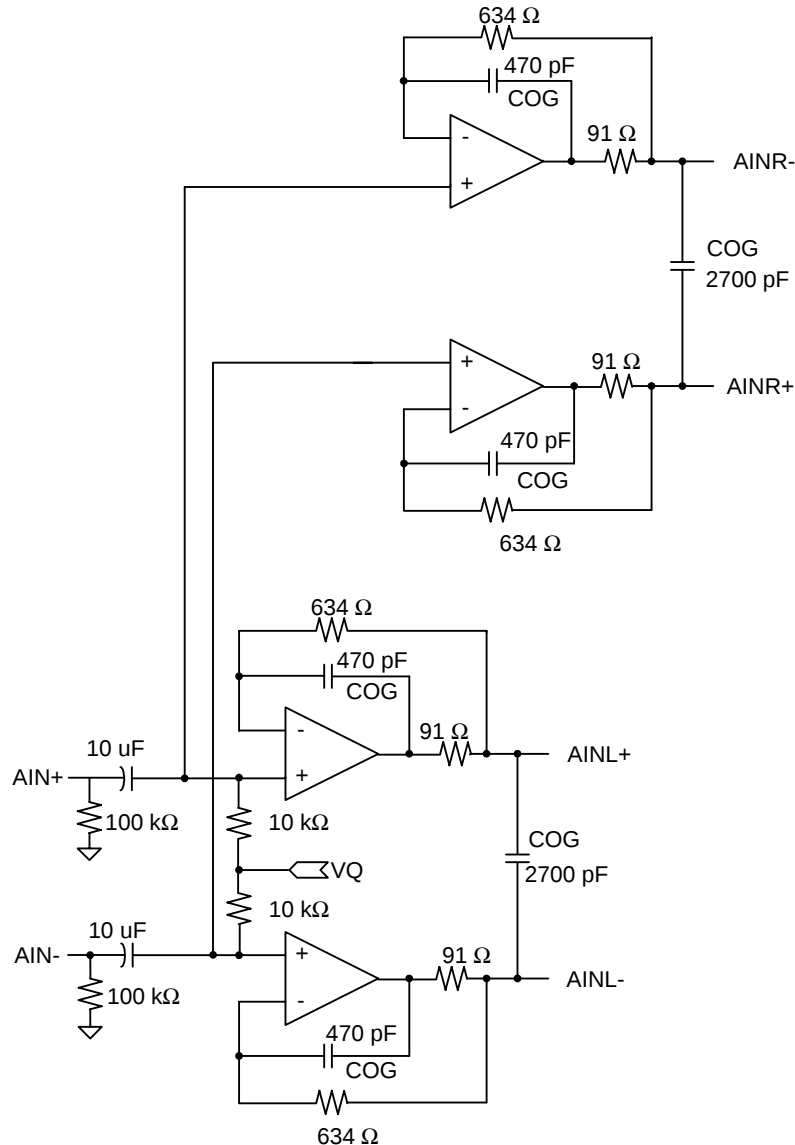


Figure 3. CS5381 Recommended Buffer Implementation for Channel Inversion

4. Demonstrating the Technique

Assembling a test system to demonstrate this technique is a relatively simple matter using standard Cirrus Logic evaluation boards and the Audio Precision System 2. The block diagram in Figure 4 shows a test set-up which includes the CDB5381 and CRD43530, the evaluation boards for the CS5381 A/D and the CS495313 audio DSP. The Audio Precision System 2 is the source of the analog signals as well as the analysis tool used to generate performance data and plots. The digital interconnections between the evaluation boards and the Audio Precision System 2 are the standard S/PDIF (IEC-60958) interface. The evaluation was performed at a 48 kHz sample rate but the performance improvement is valid at all sample rates.

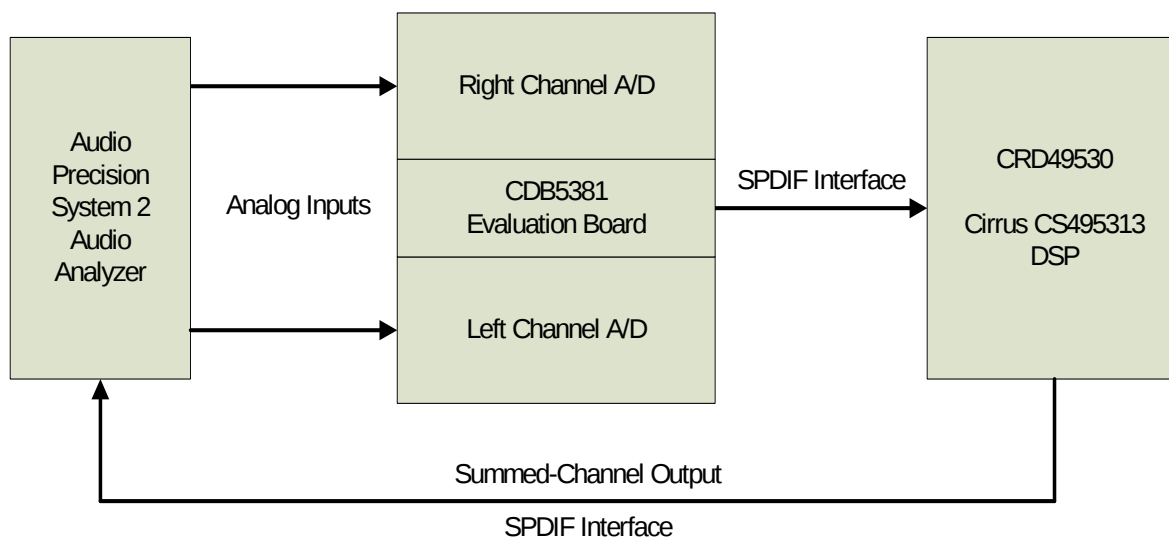


Figure 4. Test System Block Diagram

The A-weighted THD+N versus amplitude plots shown in Figure 5 clearly show the 3 dB performance improvement that can be achieved with the channel summation technique. These plots were produced with the Audio Precision generating equal amplitude and in-phase signals to both inputs of the CDB5381. The equation of $e_o = A/2 + B/2$ was performed in the DSP.

4.1 The Subtraction Approach

The analog inversion with digital subtraction technique is also easily implemented with the test system. The only differences are that the analog outputs of the Audio Precision are configured to generate an inverted signal to one of the A/D inputs and the DSP is configured implement the subtraction, $e_o = A/2 - B/2$. This configuration was tested and there was no appreciable difference between the subtraction and the addition techniques with the CS5381 in this test set-up. To a large degree, this is a result of the differential architecture of the CS5381. Implementations using different A/D architectures or systems designs have been shown to benefit from the subtraction technique and produce improved results.

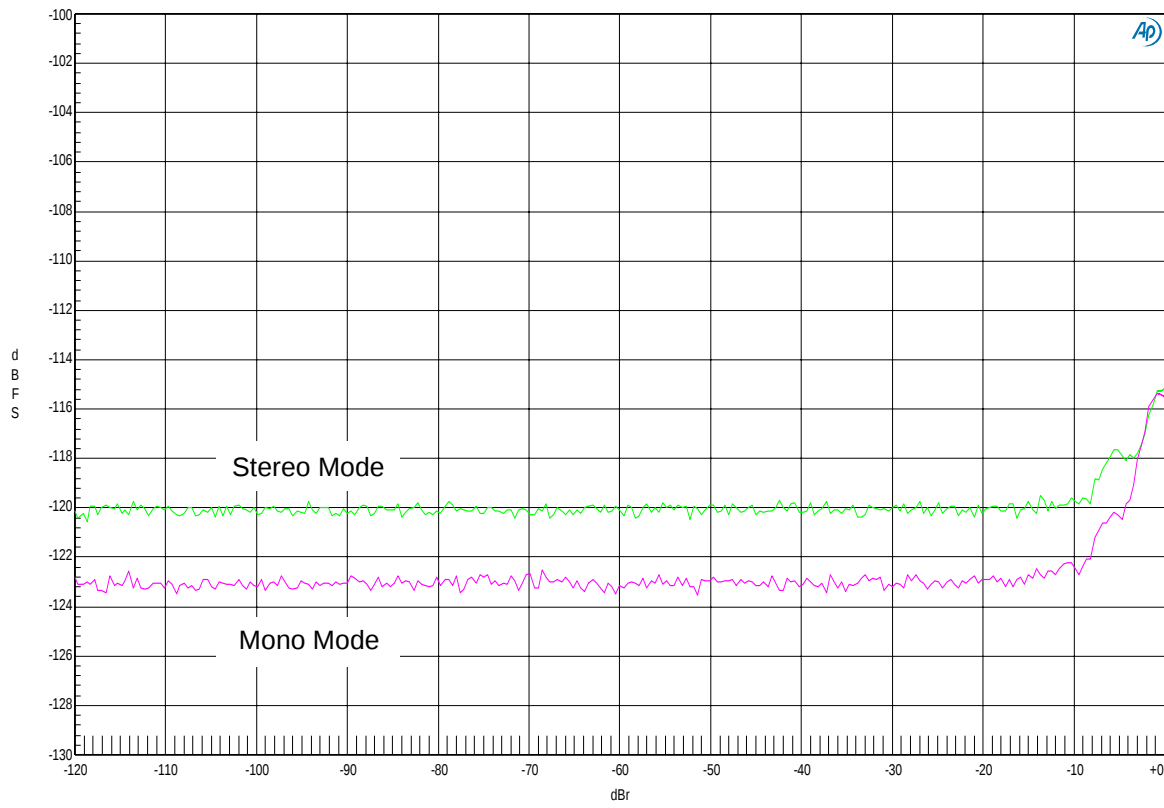


Figure 5. A-Weighted THD+N versus Amplitude at 1 kHz

Revision	Date	Changes
1	AUG 2008	Initial Release

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