AK5393 to CS5361/81 Conversion

by Kevin L Tretter

1. Introduction

The CS5361 and CS5381 are complete analog-to-digital converters for digital audio systems. They perform sampling, analog-to-digital conversion and anti-alias filtering, generating 24-bit values for both left and right channels.

The CS5361 and CS5381 offer some unique advantages over the AK5393 including:

- Over 70% REDUCTION in package size (TSSOP)
- 50% less power consumption
- 192kHz sampling capability
- Overflow detect
- Integrated level shifters
- Over 65% less group delay (48kHz output sample rate)
- External components consume less board space (See Section 2)

Table 1 shows a comparison of the key specifications of these three devices.

		AK5393	CS5361	CS5381
Conversion (Bits)		24	24	24
Dynamic Range (A-weighted)	dB	117	114	120
THD+N	dB	-105	-105	-110
Analog Core Power Supply (VA)	V	+5.0 V	+5.0 V	+5.0 V
Digital Core Power Supply (VD)		+3.3 V to +5.0 V	+3.3 V to +5.0 V	+3.3 V to +5.0 V
Digital Interface Power Supply (VL)		N/A	+2.5 V to +5.0 V	+2.5 V to +5.0 V
Maximum Power	mW	680	161	348
Maximum Sample Rate	kHz	108	200	200
Package		28-pin SOP	24-pin SOIC/TSSOP	24-pin SOIC/TSSOP

Table 1. Comparison of Key Specifications

2. Typical Connection Diagrams

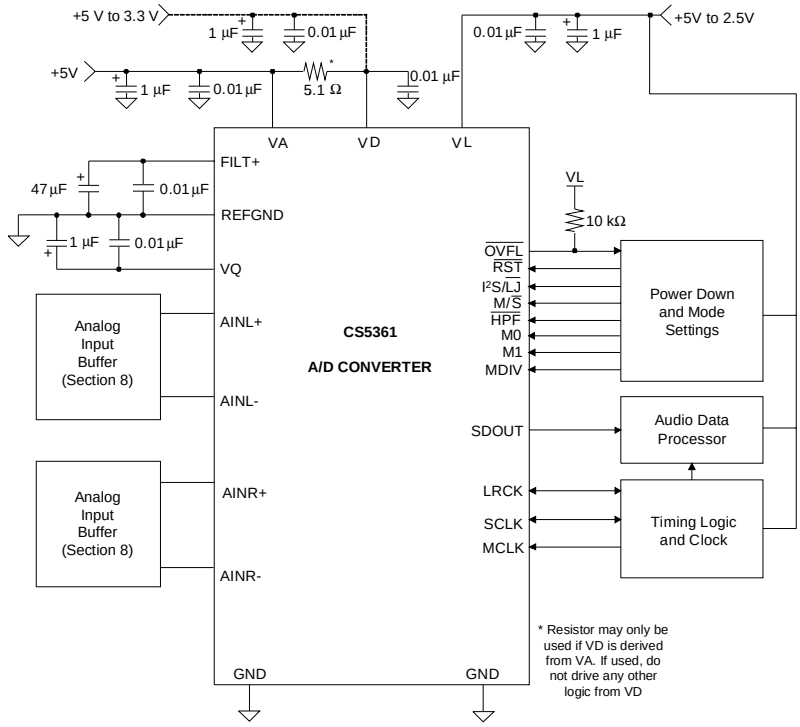

Figure 1. CS5361 Typical Connection Diagram

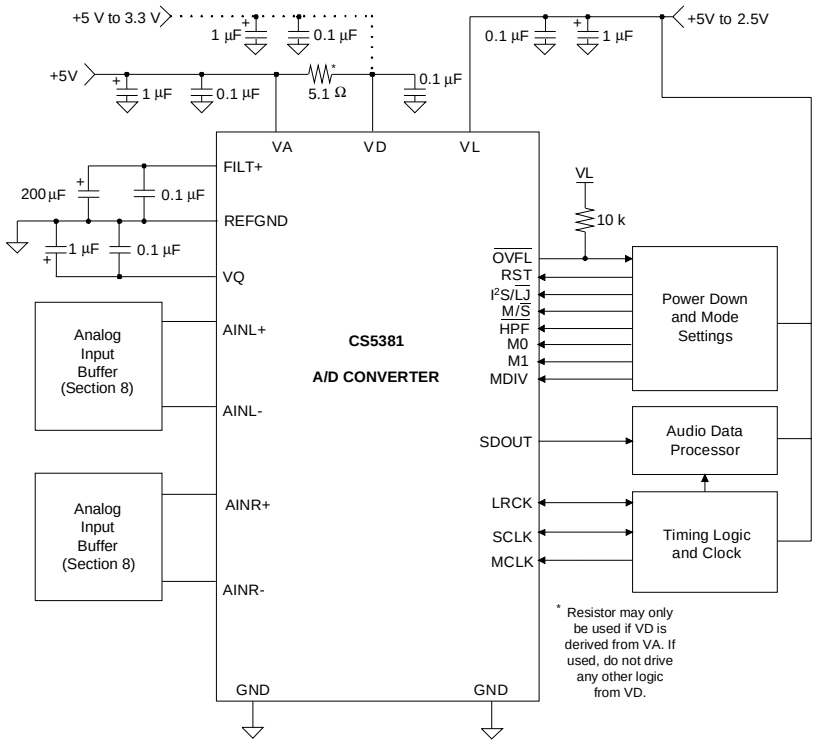

Figure 2. CS5381 Typical Connection Diagram

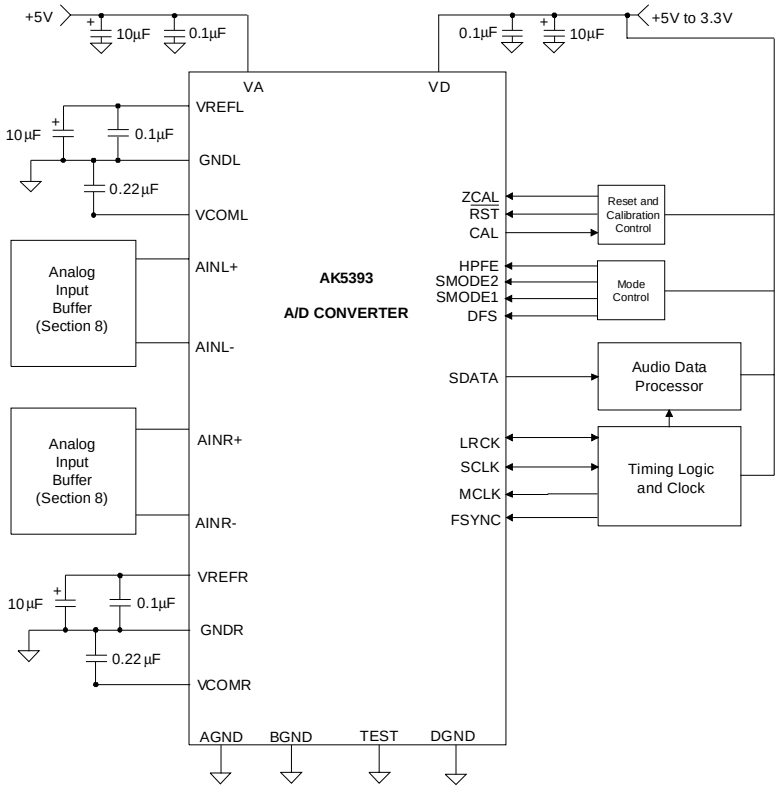

Figure 3. AK5393 Typical Connection Diagram

3. Pin Compatibility

Table 2 shows the pins of the AK5393 and the corresponding pins of the CS5361/81. Please note that the AK5393 has 28 pins, and the CS5361/81 has 24 pins.

AK5393			CS5361/81			Description
Pin Number	Pin Name		Pin Number	Pin Name		
1, 28	VREFL, VREFR		24	FILT+		Positive reference voltage
2, 27	GNDL, GNDR		23	REFGND		Ground reference
3, 26	VCOML, VCOMR		22	VQ		Internal quiescent reference voltage
4	AINL+		16	AINL+		Differential Left Channel Input
5	AINL-		17	AINL-		Differential Left Channel Input
6	ZCAL		-	-		Zero Calibration Control
7	VD		6	VD		Digital power
8	DGND		7	GND		Ground reference
9	CAL		-	-		Calibration Active Signal
10	$\overline{\text{RST}}$		1	$\overline{\text{RST}}$		Reset
11	SMODE2		12	I2S/$\overline{\text{LJ}}$		Serial Audio Interface Format Select
12	SMODE1		2	M/$\overline{\text{S}}$		Master/Slave Mode Select
13	LRCK		3	LRCK		Left right clock
14	SCLK		4	SCLK		Serial clock
15	SDATA		9	SDOUT		Serial data
16	FSYNC		-	-		Frame Synchronization Signal
17	MCLK		5	MCLK		Master clock
18	DFS		13	M0		Mode Selection
19	HPFE		11	$\overline{\text{HPF}}$		High Pass Filter Enable
20	TEST		-	-		Test
21	BGND		-	-		Substrate Ground
22	AGND		18	GND		Ground reference
23	VA		19	VA		Analog power
24	AINR-		20	AINR-		Differential Right Channel Input
25	AINR+		21	AINR+		Differential Right Channel Input
			14	M1		Mode Selection
			8	VL		Logic Power
			10	MDIV		MCLK divider
			15	$\overline{\text{OVFL}}$		Overflow

Table 2. Pin Compatibility Between AK5393 and CS5361/81

4. Offset Calibration

The CS5361, CS5381, and AK5393 all have offset calibration capability. However, the calibration process varies slightly between the AK5393 and the CS5361/CS5381.

4.1 CS5361 and CS5381

The CS5361 and CS5381 implement a high pass filter that can be controlled via the $\overline{\text{HPF}}$ pin (pin 11). The high pass filter continuously subtracts a measure of the DC offset from the output of the decimation filter. If the $\overline{\text{HPF}}$ pin is taken high during normal operation, the current value of the DC offset register is frozen and this DC offset will continue to be subtracted from the conversion result.

A system calibration can then be performed by first running the CS5361 or CS5381 with the high pass filter enabled ($\overline{HPF}$ = LOW) until the filter settles. At this point, disable the high pass filter ($\overline{HPF}$ = HI), thereby freezing the stored DC offset.

4.2 AK5393

The AK5393 will automatically initiate a calibration sequence following a reset. The CAL pin (pin 9) is an output that indicates when a calibration sequence is in progress. This calibration technique is very similar to that described above for the CS5361 and CS5381.

The AK5393 also has a ZCAL pin (pin 6) which allows the calibration input to be obtained from either the analog input pins or the VCOM pins. The high pass filter can be controlled via the HPFE pin (pin 19). In the AK5393, the high pass filter is either continuously running or completely removed from the signal path.

5. Master/Slave Selection and Digital Interface Format

The CS5361, CS5381, and AK5393 are pin compatible in terms of selecting Master/Slave operation and digitial interface format. The pins match up as noted in Table 2.

6. Speed Mode Selection

The AK5393 supports two speed modes, “normal” and “double” as determined by the DFS pin (pin 18). This pin is compatible with the M0 pin (pin 13) of the CS5361 and CS5381, as shown in Table 2. In this case, the M1 pin (pin 14) of the CS5361 and CS5381 must be tied low.

7. System Clocking

The CS5361 and CS5381 are fully compatible with the clocking requirements of the AK5393. However, there is a slight difference when operating in Master mode. If DFS = LOW, the AK5393 will generate an SCLK that is $128\times F_S$. The CS5361 and CS5381 generate an SCLK that is $64\times F_S$.

The CS5361 and CS5381 offer an integrated MCLK divider, which can be controlled via the MDIV pin (pin 10). This pin allows multiple external MCLK/LRCK ratios to be supported. In order to maintain complete compatibility between the AK5393 and the CS5361/CS5381, connect the MDIV pin (pin 10) of the CS5361/CS5381 to GND.

8. Input Buffer Topology

The analog input buffers shown in Figures 7 and 8 of the AK5393 datasheet (dated April, 2000) will also work for the CS5361/81. In this case, the “*Bias*” reference should be sourced from the VQ pin of the CS5361/81. However, these input buffers require a large input voltage level at the input to the buffer and attenuate the signal prior to the converter. This much signal swing is not always possible in a real system, and not necessary to achieve the full performance of the CS5361 and CS5381.

The following sections contain a description of a single-ended to differential input buffer (comparable to Figure 7 of the AK5393 datasheet) and a fully differential input buffer (comparable to Figure 8 of the AK5393 datasheet). These two buffer topologies are unity gain, and therefore do not rely on a large input voltage at the buffer input.

8.1 Single-Ended to Differential Input Buffer

Figure 4 shows a single-ended to differential analog input buffer. This buffer provides the proper biasing, isolation from the switched capacitor currents, low output impedance, and anti-alias filtering. The second op-amp stage is set up in an inverting configuration to produce the negative node of the differential input. In the input buffer shown below, the second stage has unity gain, and the single-ended input level will effectively be doubled when presented differentially to the converter. For example, a 2.8 Vpp single-ended input will provide a full-scale 5.6 Vpp differential input to the CS5361/CS5381.

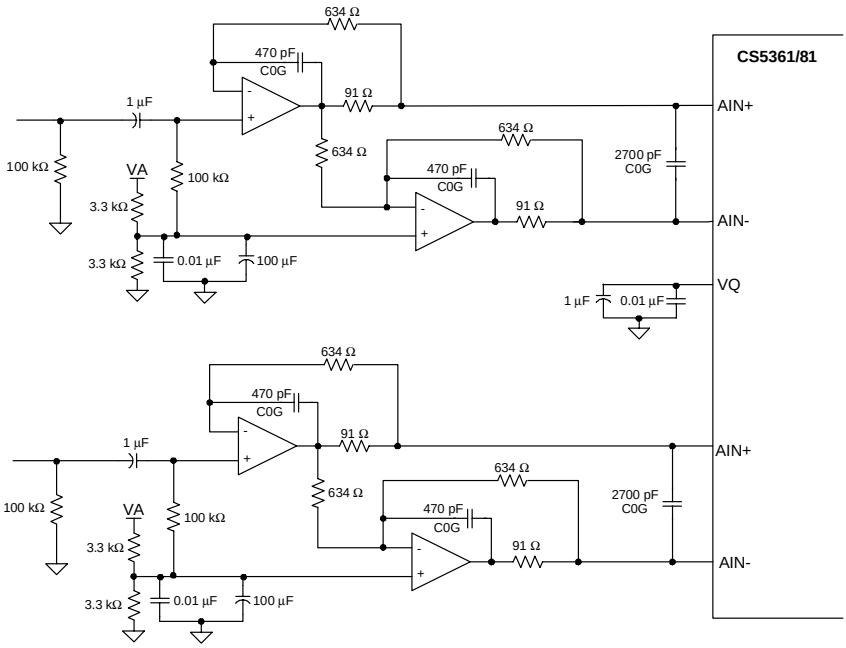

Figure 4. Single-Ended to Differential Input Buffer

8.2 Fully Differential Input Buffer

Figure 5 shows a fully differential analog input buffer. This buffer provides the proper biasing, isolation from the switched capacitor currents, low output impedance, and anti-alias filtering. This input buffer is unity gain, so a 5.6 Vpp differential input will provide a full-scale 5.6 Vpp differential input into the CS5361/CS5381.

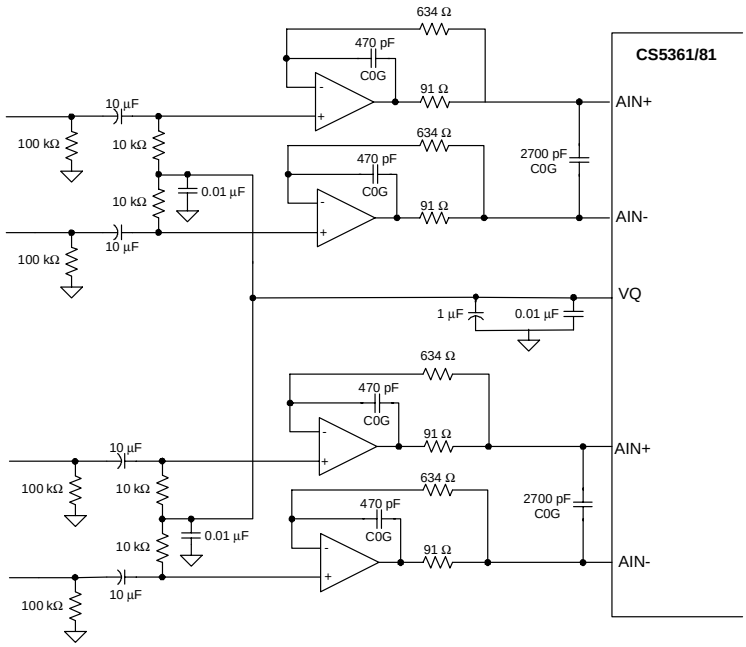

Figure 5. Fully Differential Input Buffer

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